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# MS-7918 Ver: 1.0

ATX (243.84x304.8) mm

## Intel Haswell Refresh Platform

### CPU:Socket H3

2013 Haswell  
2014 Boardwell

### PCH:FCBGA708

Z97/H97/B85  
SPI ROM: 64 MB  
128 MB (H97/B85)

### Main Memory:

Dual Channel DDR3 \* 4 (Max 32G)

### Power Solution:

Vcore : UP1649 6 Phase  
DDR : UP1504

### ACPI:

UPI

### Onboard Chip:

LAN : Killer E2205  
PCI Brige : ASM1083  
HD Codec:ALC1150 + AMP  
(Gaming Type)  
SIO:Nuvoton 6792D

### Expansion Slots:

PCI Express (X16) Slot \* 1  
PCI Express (X1 ) Slot \* 2  
PCI Express (X4 ) Slot \* 1 ➤ (Share Bandwidth)  
PCI Slot \* 3  
M.2 Slot (Socket 3) \* 1 (Share SATA)



### Internal Connectors

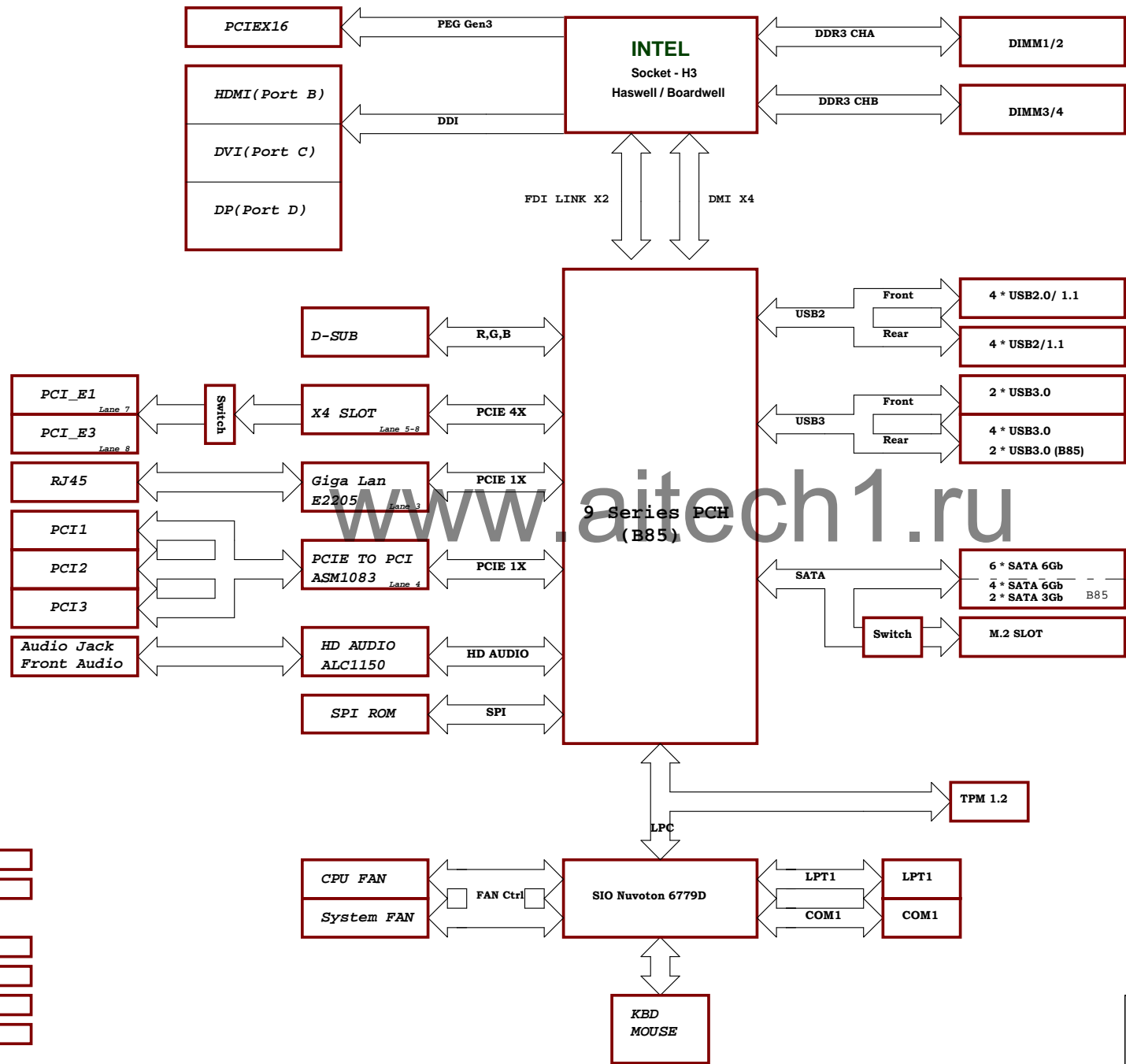
SATA Gen3 \* 6  
FUSB2 Header \* 2  
FUSB3 Header \* 1  
Front Audio Header \* 1  
Serial Port Header \* 1  
Parallel Port Header \* 1  
Front Panel Header \* 2  
SPI Header \* 1  
TPM Header \* 1  
CPU Fan \* 2  
System Fan \* 2

### Real I/O Connectors

PS2 + Dual USB2  
Dual USB3 (B85 USB2)  
DSUB + DVI  
DP + HDMI + SPDIF  
RJ45 + Dual USB3  
Audio Jack 6 Port

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Block Diagram



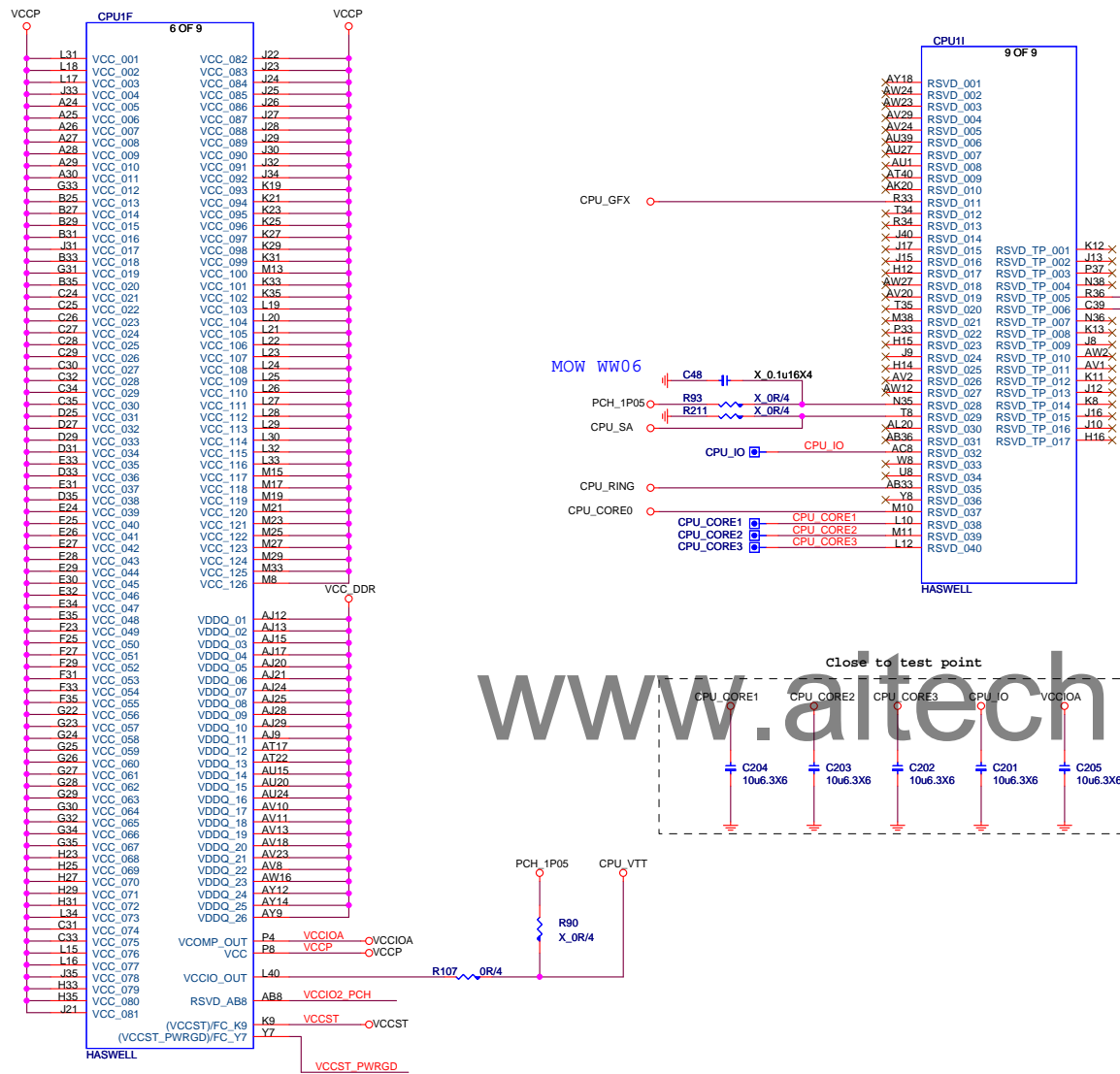
Slot Sequence:

PCIEX16	M.2 Slot
PCIEX16	
PCIEX16	
PCI SLOT	
PCIEX16(X4)	
PCI SLOT	
PCI SLOT	





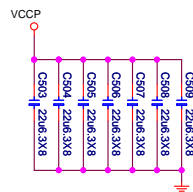




Close to test point

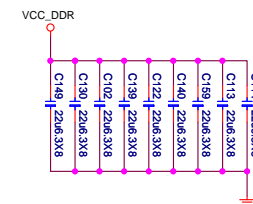
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## +CPU\_VCCP-Decoupling



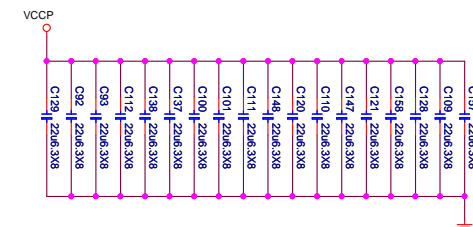
PLACE 0805 CAPS IN CPU SOCKET BOTTOM

## +1.5V\_DDR3-Decoupling



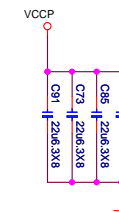
CPU SOCKET CAVITY 0805CAPS

## +CPU\_VCCP-Decoupling



PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

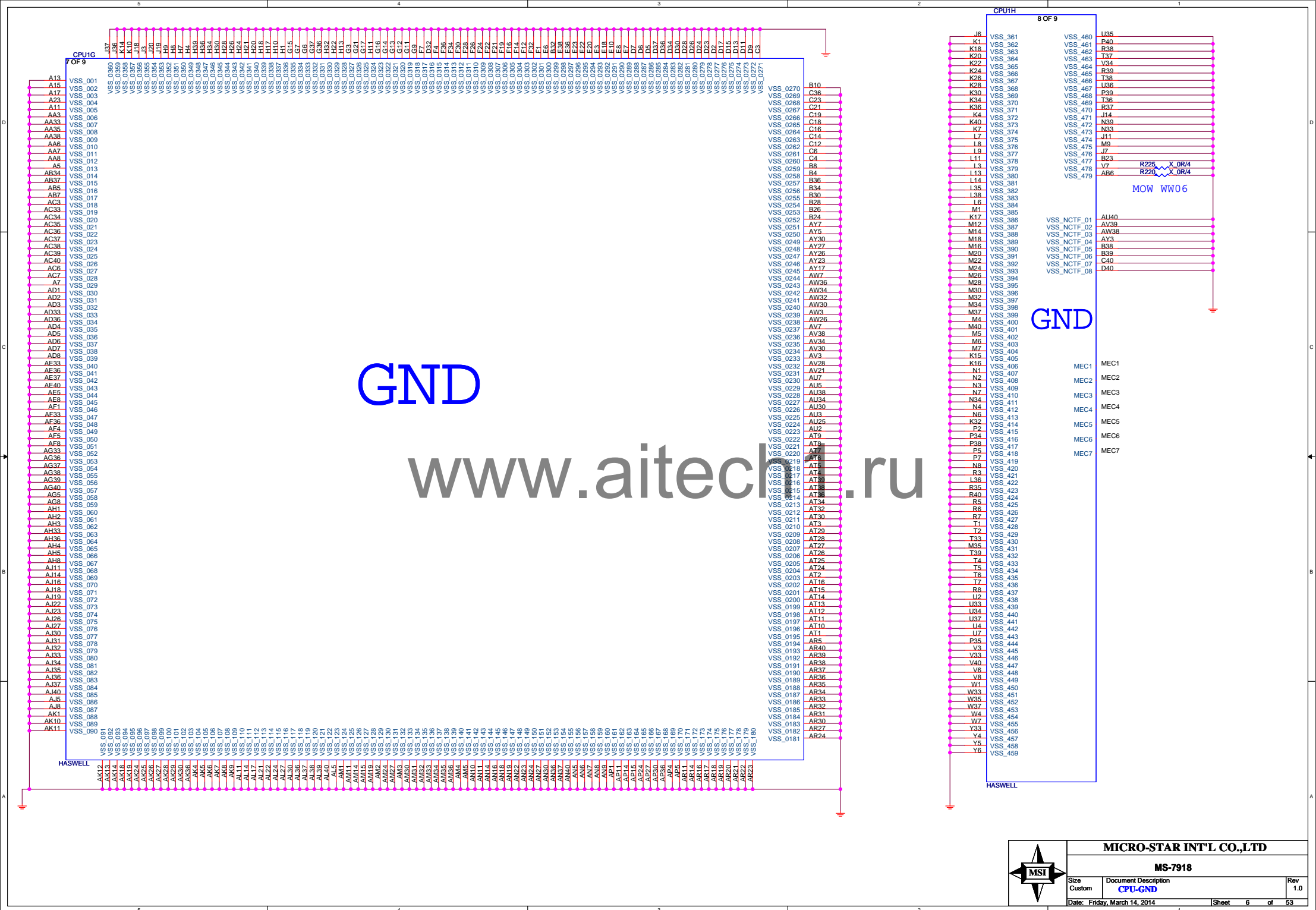
PLACE 0805CAPS Near CPU SOCKET edge



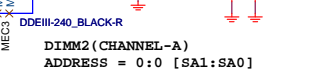
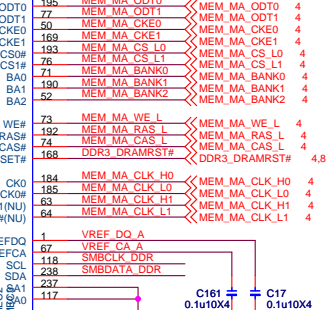
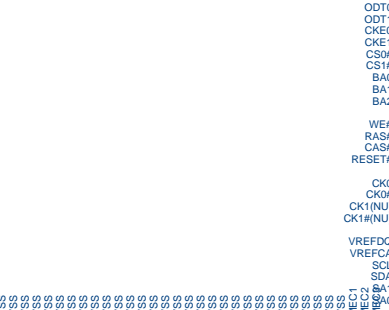
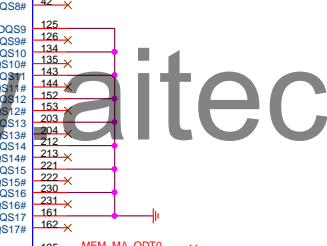
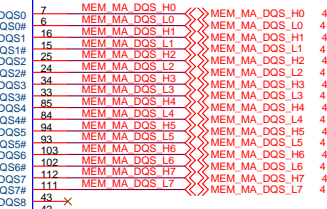
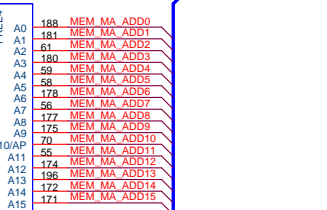
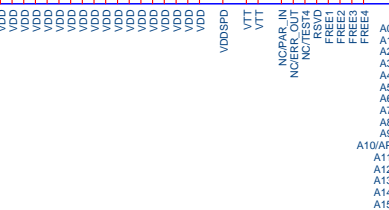
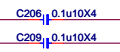
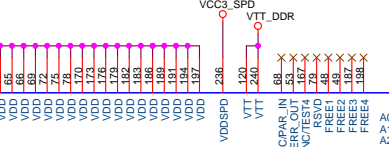
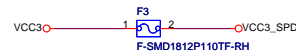
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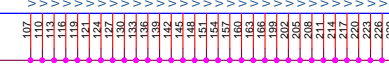
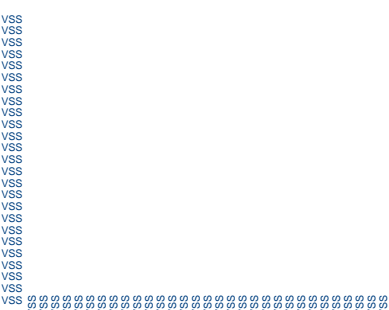
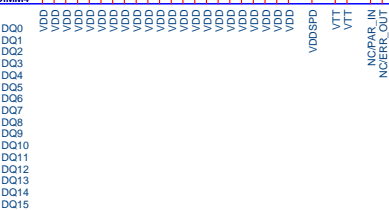
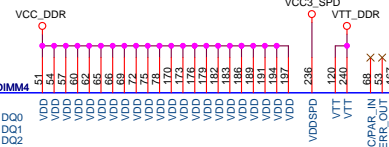
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## DDRIII DIMM\_A0

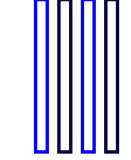


## DDRIII DIMM\_A1

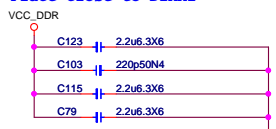


Address	Instruction	Comment
00000000	MEM MA DATA47	216 DO46
00000001	MEM MA DATA48	99 DO47
00000002	MEM MA DATA49	100 DO48
00000003	MEM MA DATA50	105 DO49
00000004	MEM MA DATA51	106 DO50
00000005	MEM MA DATA52	218 DO51
00000006	MEM MA DATA53	219 DO52
00000007	MEM MA DATA54	224 DO53
00000008	MEM MA DATA55	225 DO54
00000009	MEM MA DATA56	225 DO55

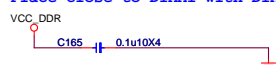
A0 A1 B0 B1



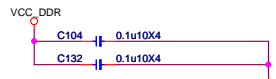
Place close to DIMM1



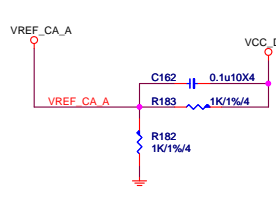
Place close to DIMM1 with DIMM2



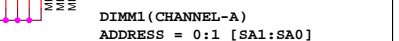
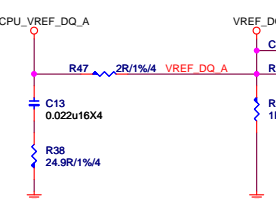
Place close to DIMM2



## UPI VOLTAGE CONSOLE



## UPI VOLTAGE CONSOLE

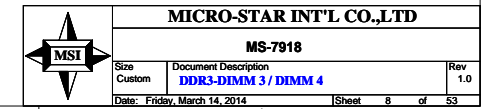


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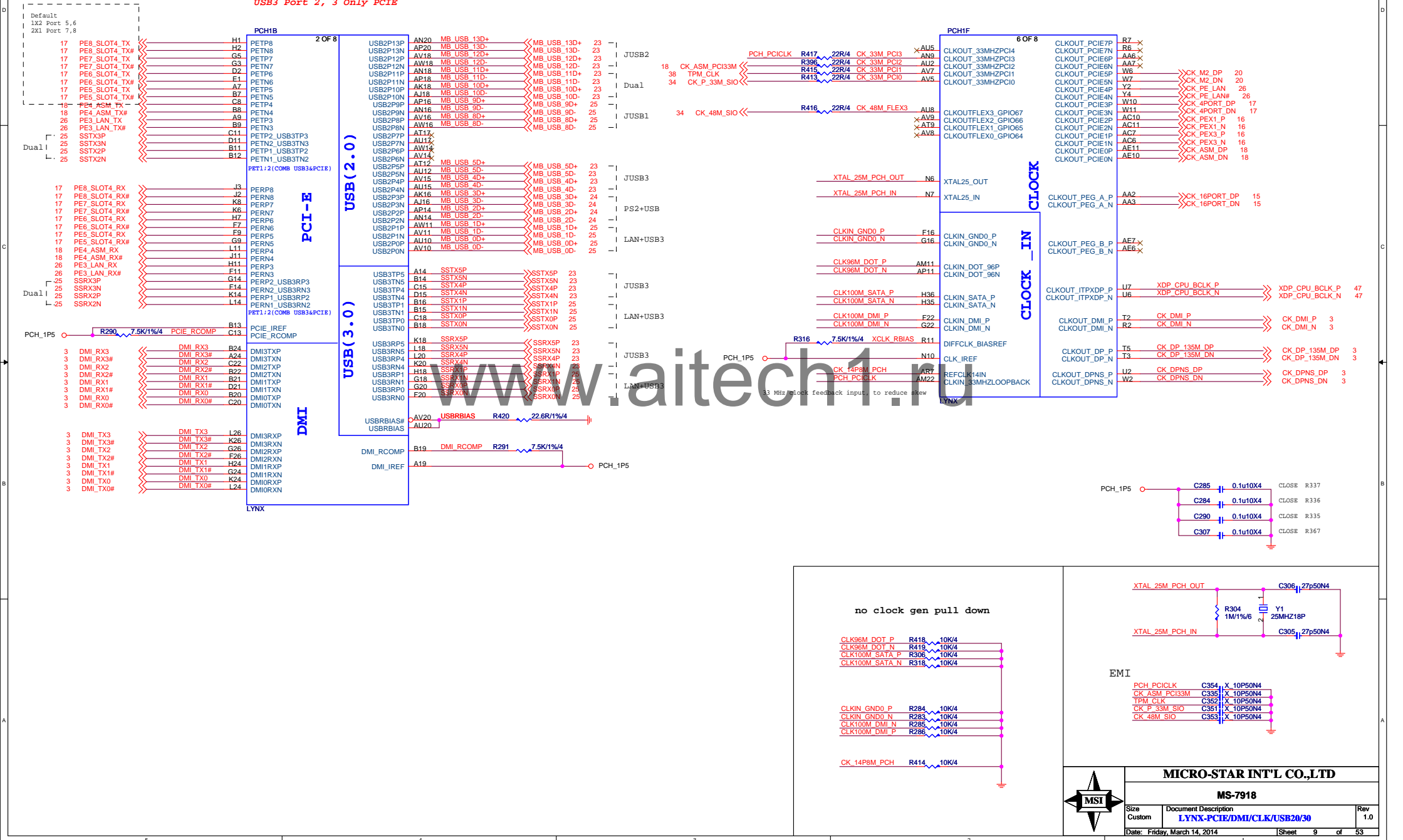
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## DDRIII DIMM\_B1



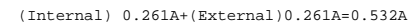
B85  
USB2 Port 6,7 Disable  
USB3 Port 2, 3 Only PCIE



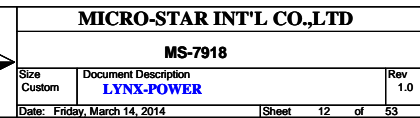
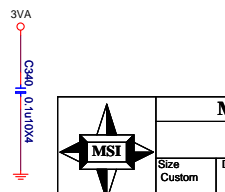
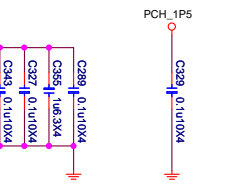
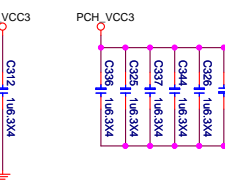
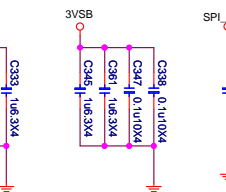
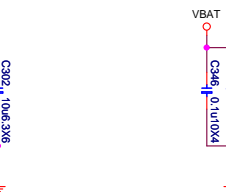
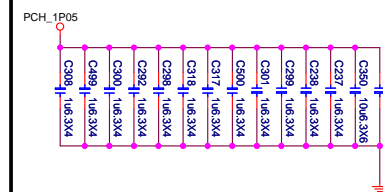


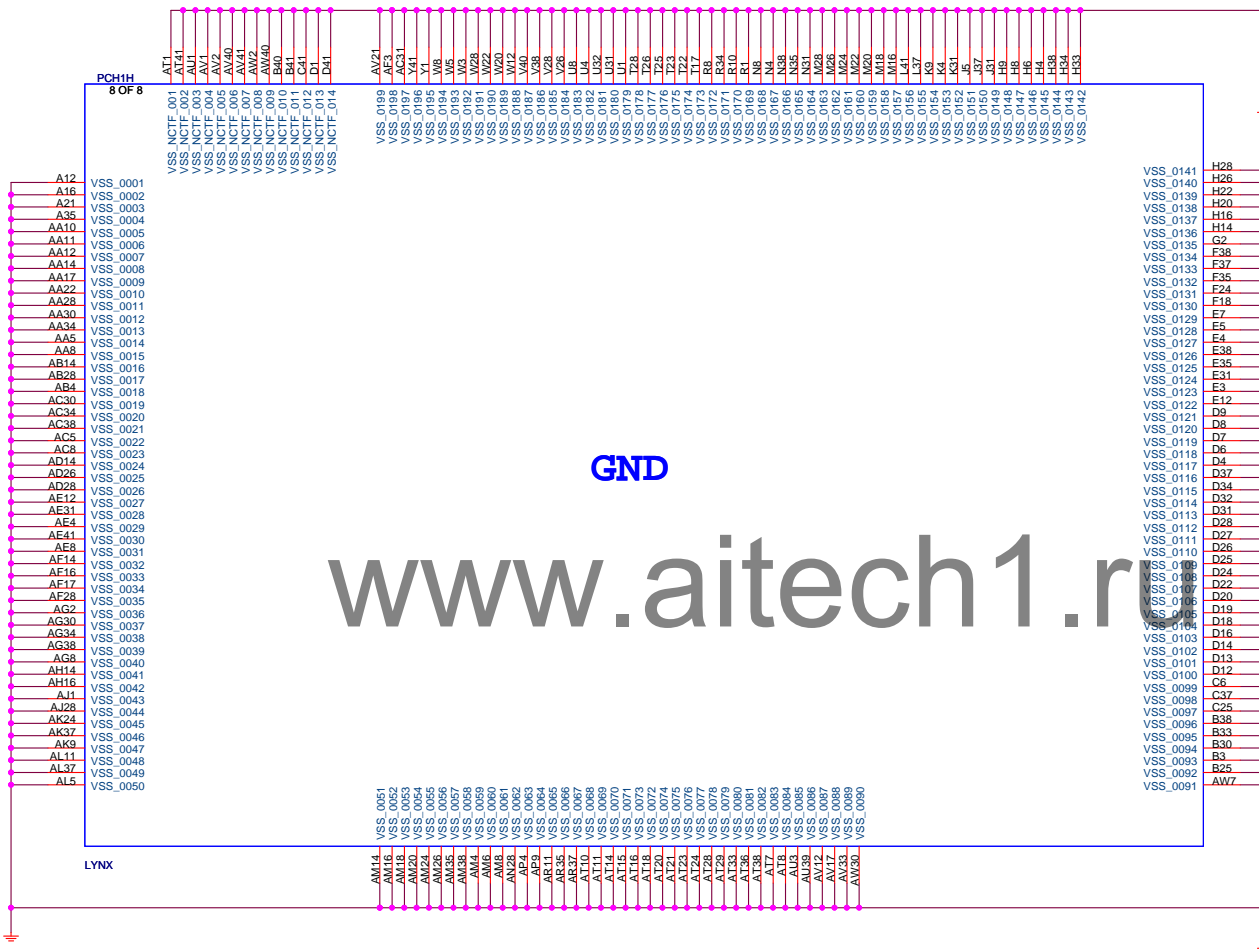


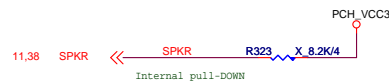


$$(\text{Internal}) \ 1.29A + (\text{External}) \ 1.12A = 2.41A$$


PCH\_1P5 3VA

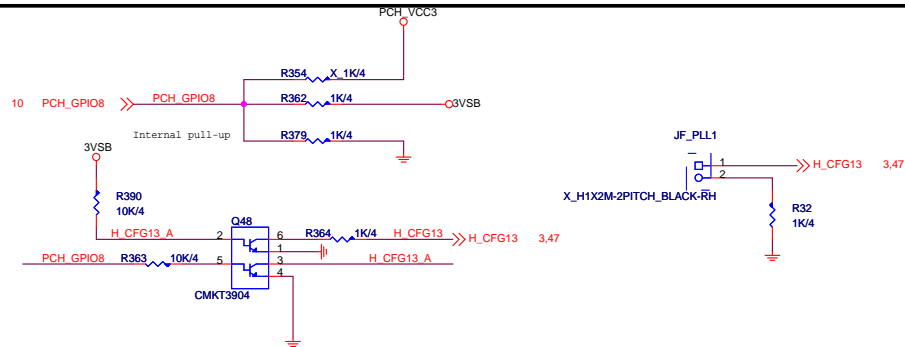
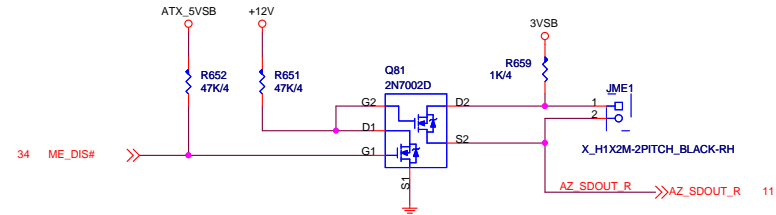






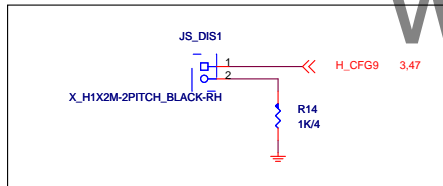
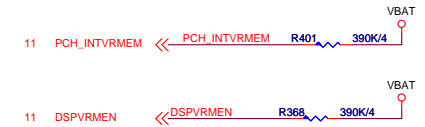
**SPKR**  
Default Mode:  
Internal weak Pull-down.

No Reboot Mode with TCO Disabled:  
Connect to Vcc3\_3 with 8.2k-10k Ohm weak pullup resistor.

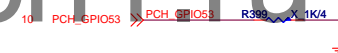


**PCH\_GPIO55**  
Default Mode:  
Internal pull-up.

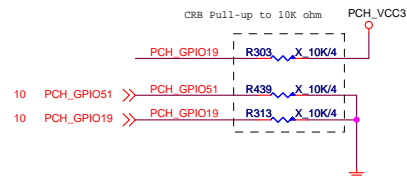
Top Block Swap Mode:  
Connect to ground with 4.7k Ohm weak pulldown resistor.



**PCH\_GPIO53**  
Connect to ground with 1k Ohm pull-down resistor.



For Sx power Cycling May Fail Due to SVID Logic Race Condition Within the Processor



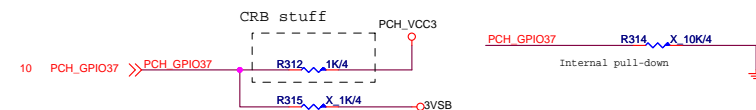
Default (SPI):  
Left both SATA1GP/GPIO19 and GPIO51 floating.  
No pull up required.

Boot from PCI:  
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.  
Leave GPIO51 Floating.

Boot from LPC:  
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

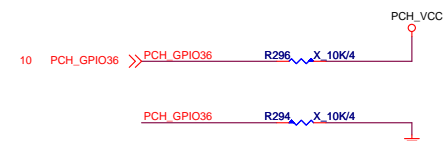
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default



Enable TLS:  
Pull up with 1k Ohm to VccSus3.3.

Default (Disable TLS):  
Leave NC. Internal pull down.



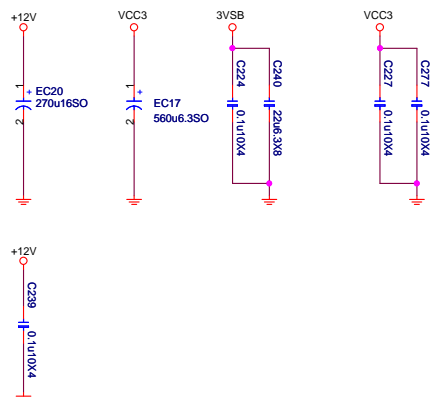
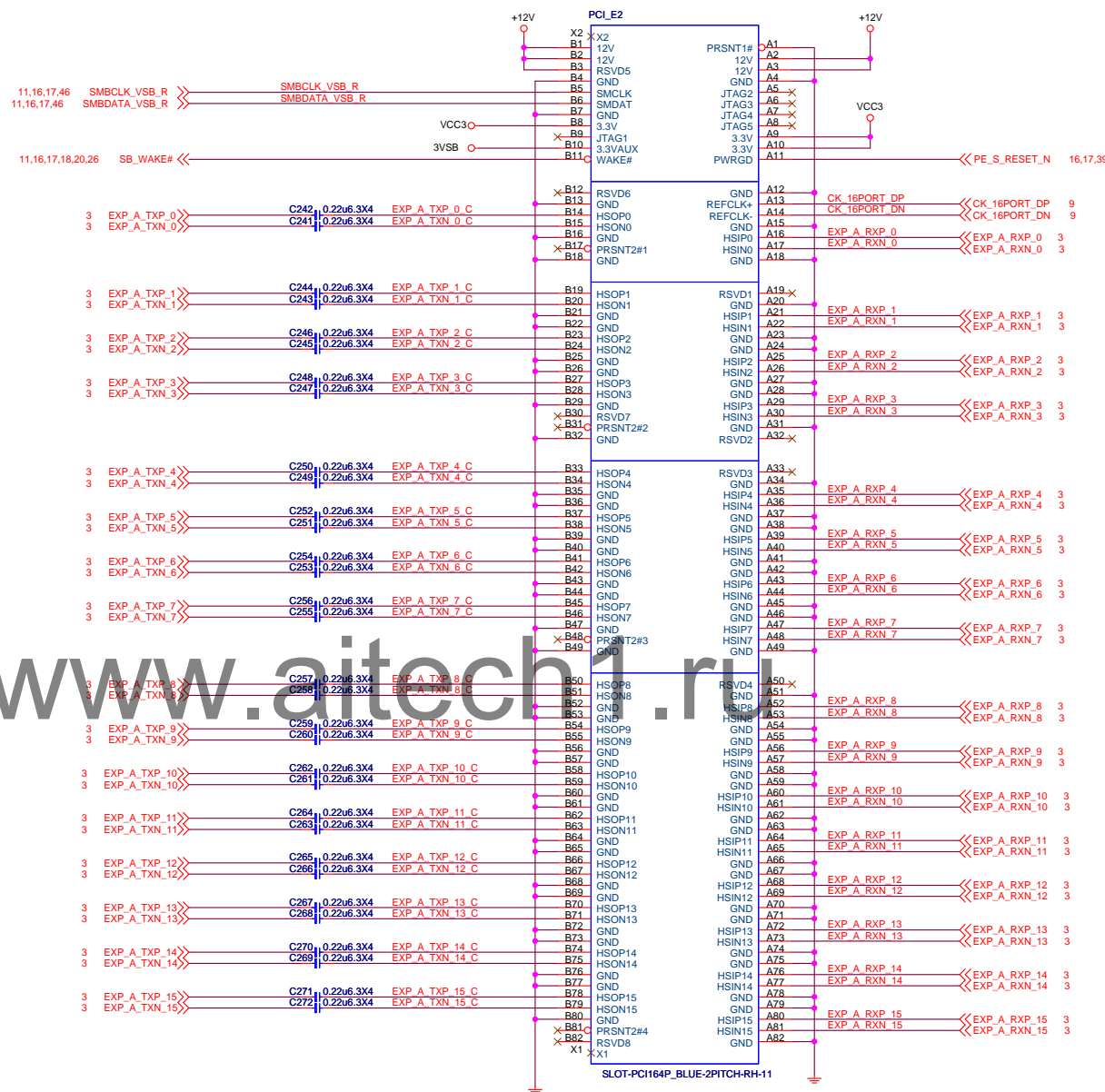
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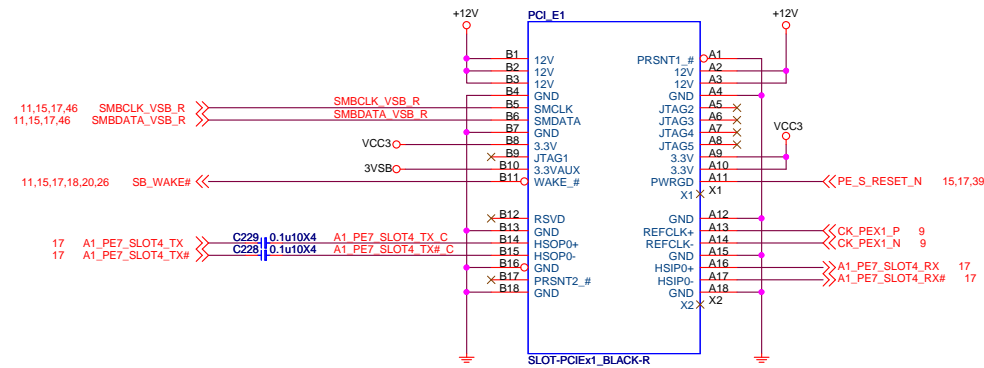
12V - 5.5A  
VCC3 - 3A  
3VSBV - 375mA



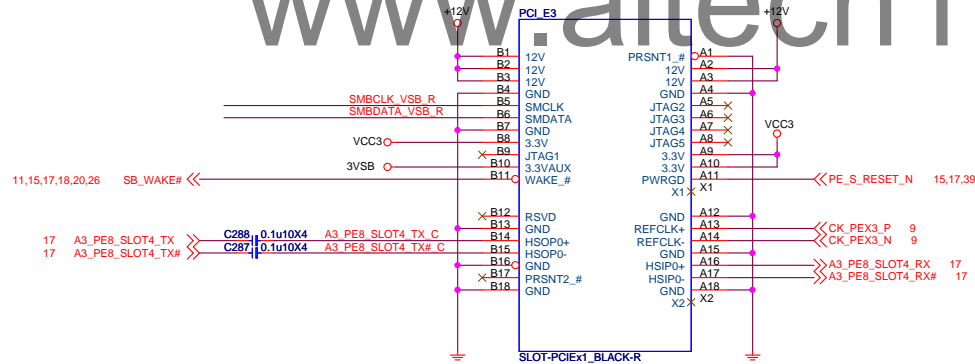
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12V - 0.5A  
VCC3 - 3A  
3VSBV - 375mA



12V - 0.5A  
VCC3 - 3A  
3VSBV - 375mA

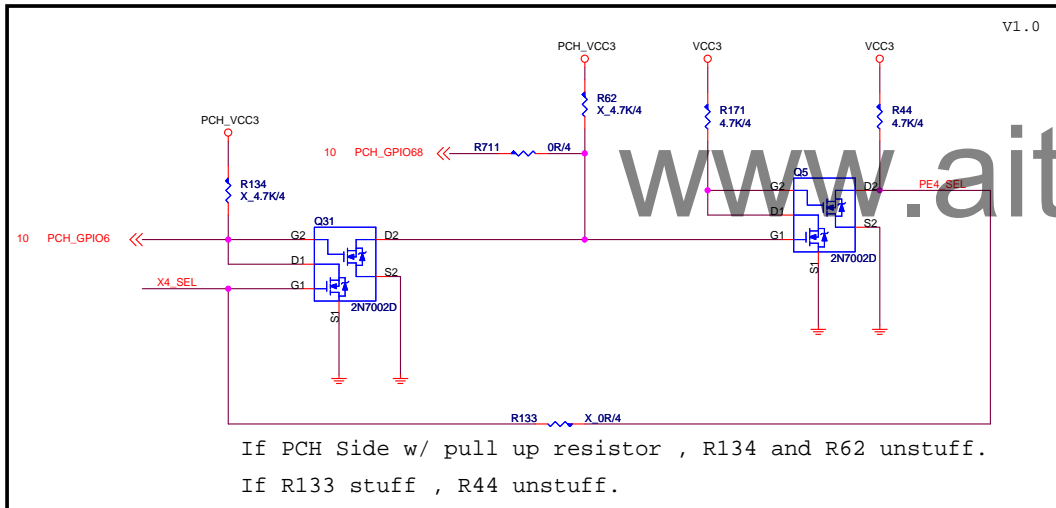
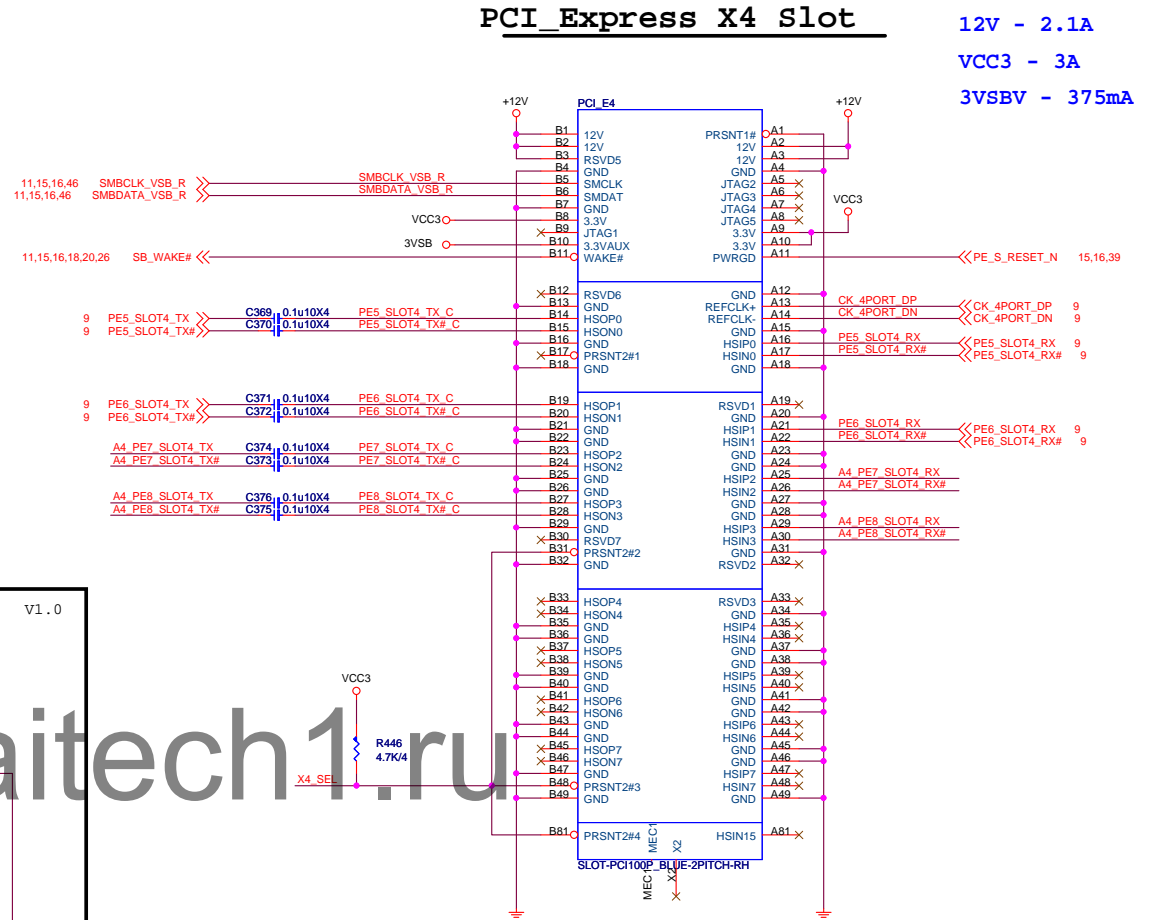
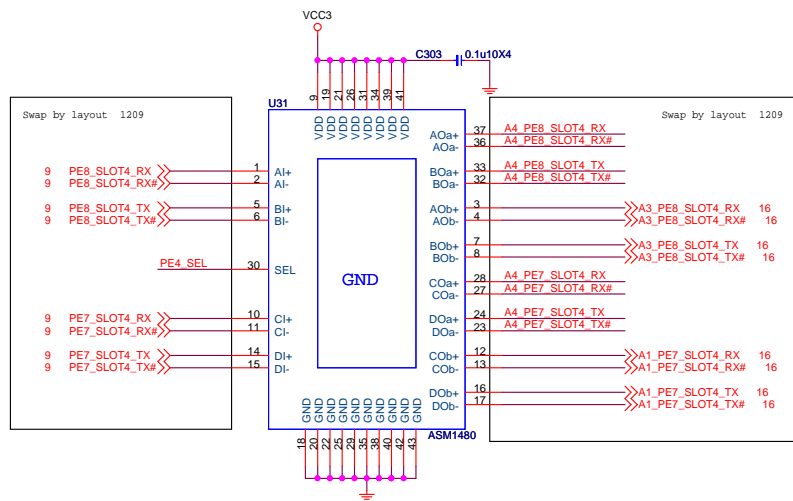
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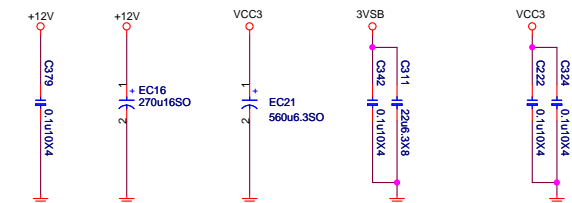
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Custom	PCIE SLOT (X1)	1.0
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If PCH Side w/ pull up resistor , R134 and R62 unstuff.  
If R133 stuff , R44 unstuff.

Default PCI\_E1,PCI\_E3,PCI\_E4 Working

	HW		SW	
	X2+1+1	X4	2+1+1	X4
X4_SEL	High	Low	X	X
PCH_GPIO6	Low	High	Low	Low
PCH_GPIO68	High (GPI)	Low (GPI)	High (GPO)	Low (GPO)



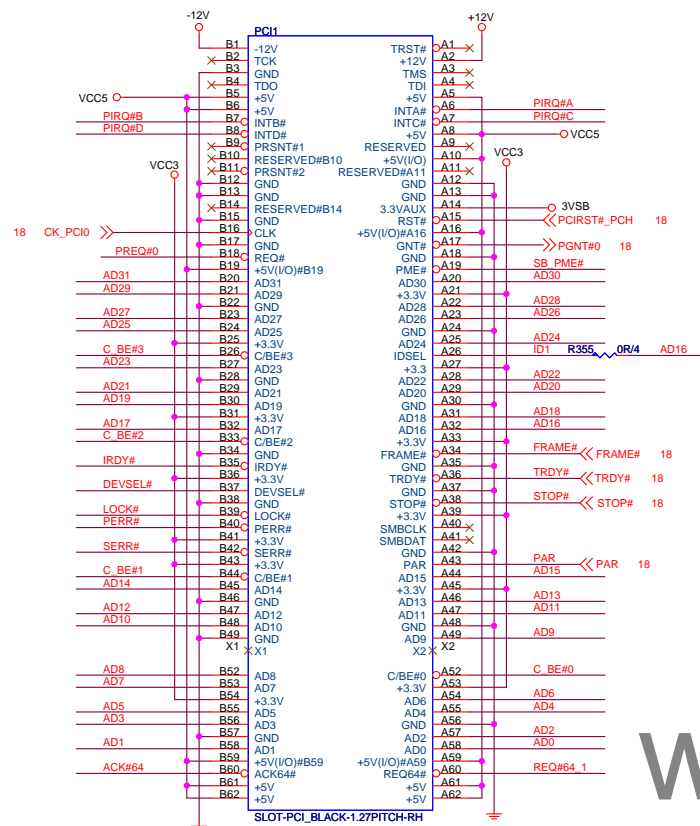
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**MS-7918**

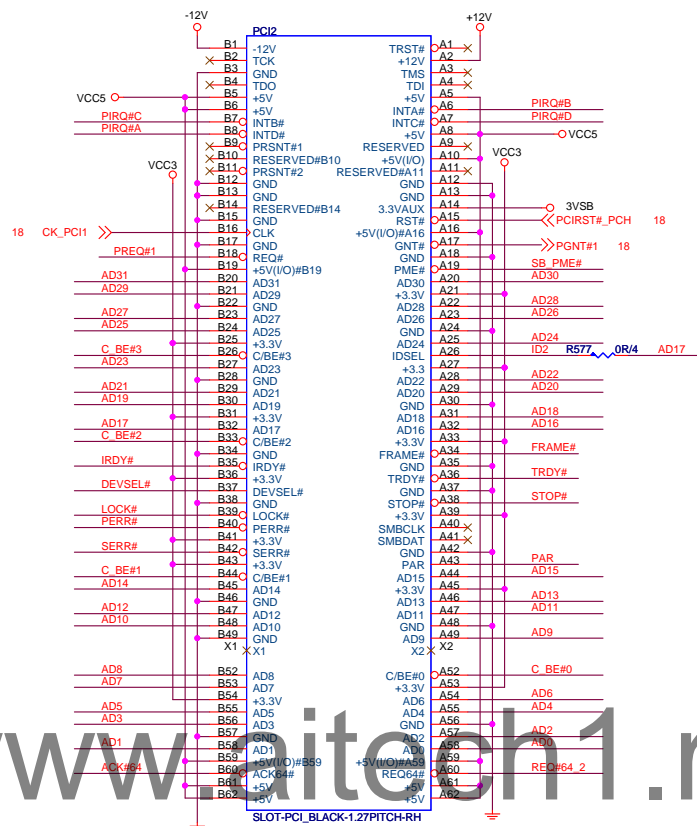
Size Custom Document Description **PCIE SLOT (X4)** Rev 1.0

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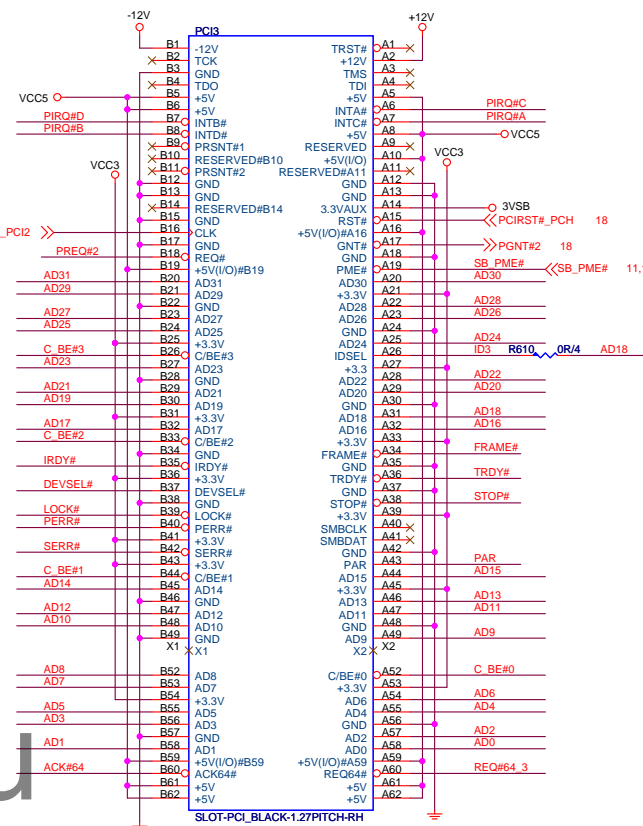




**IDSEL = AD16**  
**MASTER = PREQ#0**  
**PIRQ#A**



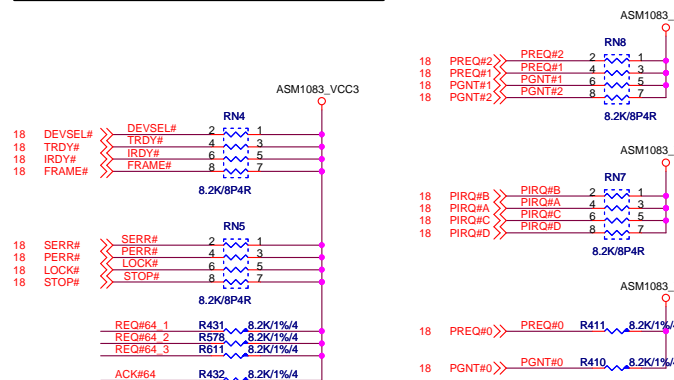
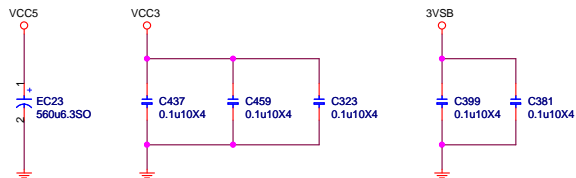
**IDSEL = AD17**  
**MASTER = PREQ#1**  
**PIRQ#B**



**IDSEL = AD18**  
**MASTER = PREQ#2**  
**PIRQ#C**

#### PCI PULL-UP / DOWN RESISTORS

AD[31..0] <<> AD[31..0] 18  
 C\_BE[3..0] <<> C\_BE[3..0] 18



#### PCI slot (X3)

+3.3Vaux (wake)	- 1125mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 15A
+12V	- 1.5A



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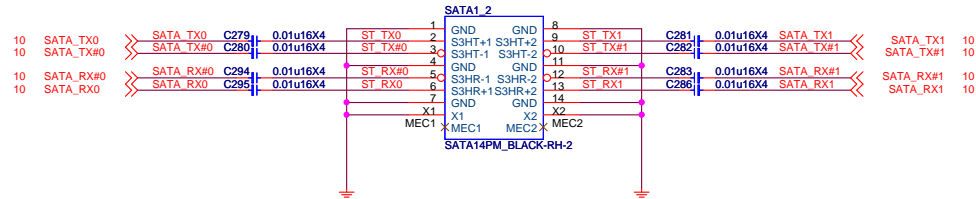
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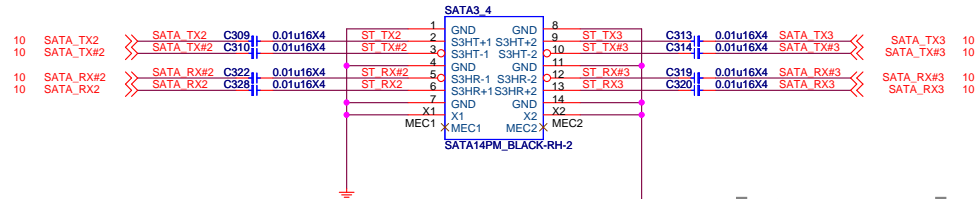
### SATA 6G PORT 0,1

Gaming Black



### SATA 6G PORT 2,3

Gaming Black

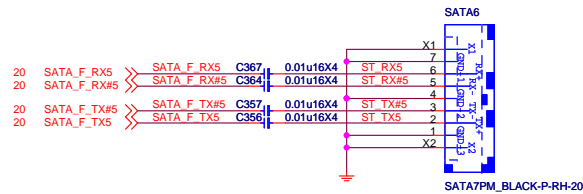
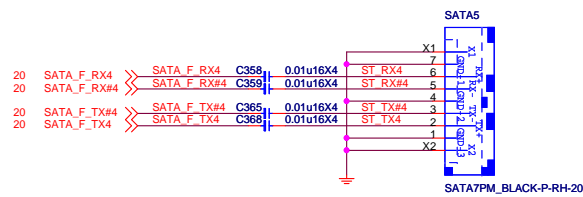


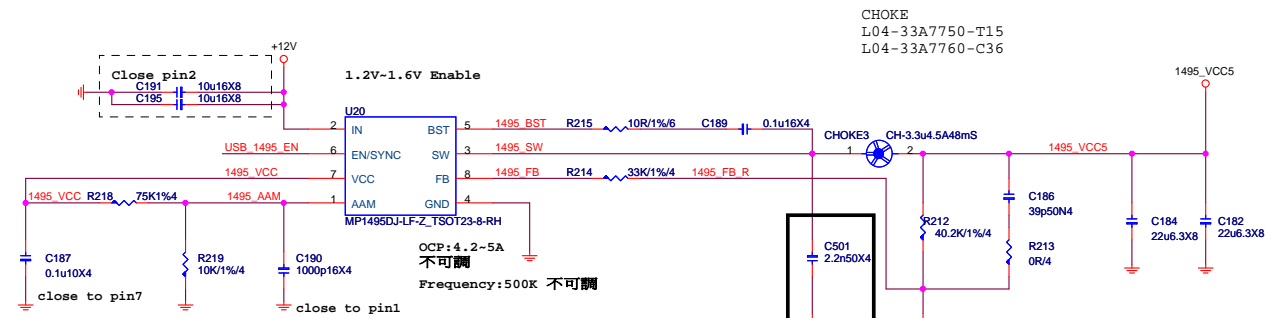
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### SATA 6G PORT 0,1

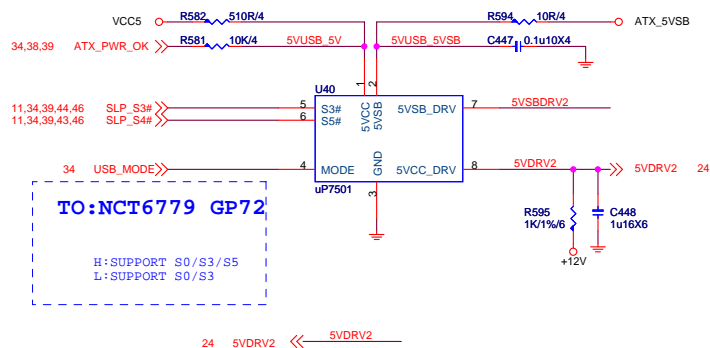
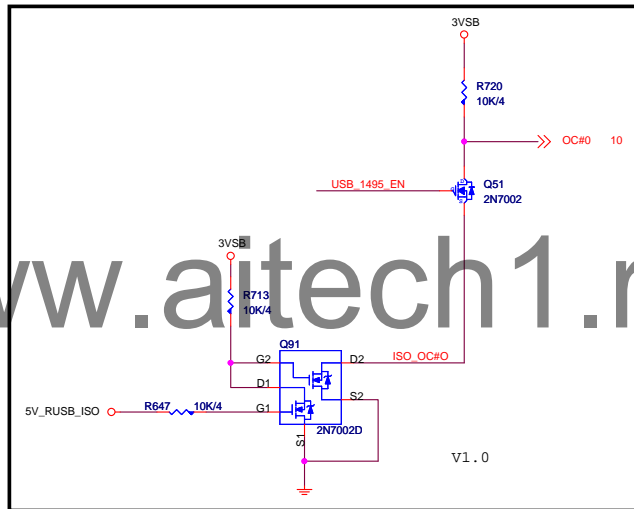
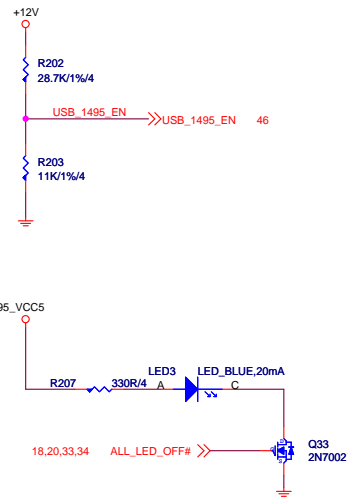
Gaming Black

Z97/H97 SATA Gen3  
B85 SATA Gen2

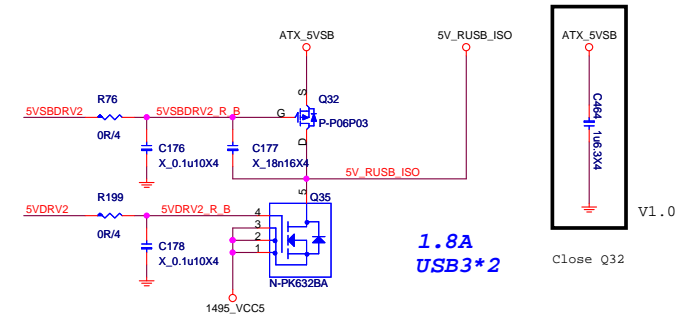




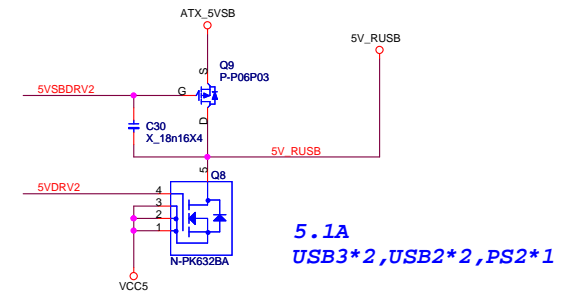
CHOKER  
L04-33A7750-T15  
L04-33A7760-C36



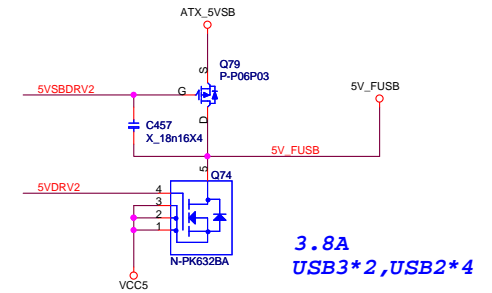
## LAN\_USB PORT POWER



## Real USB PORT POWER

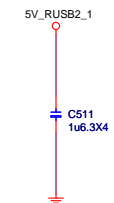
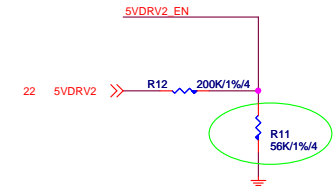


## Front USB PORT POWER





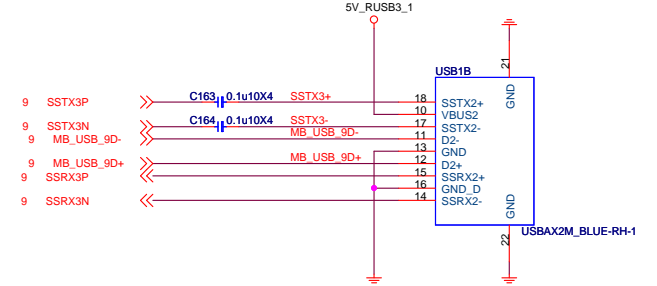
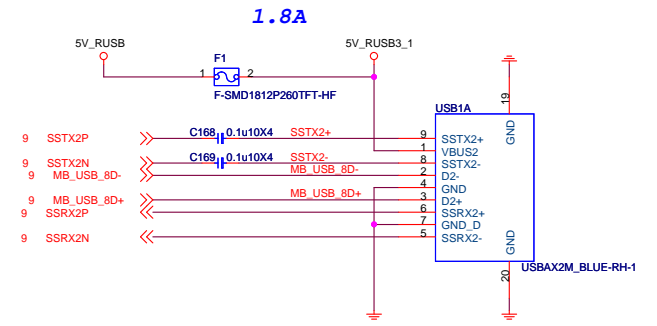
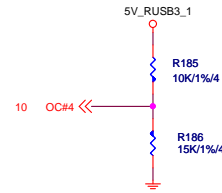
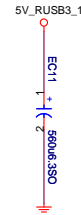
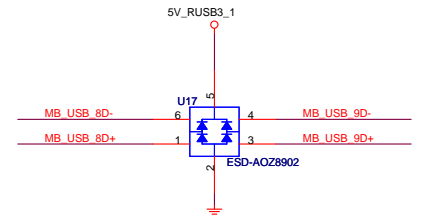
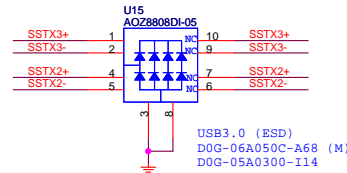
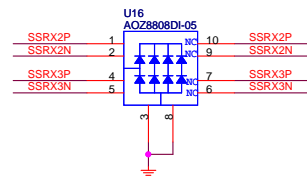
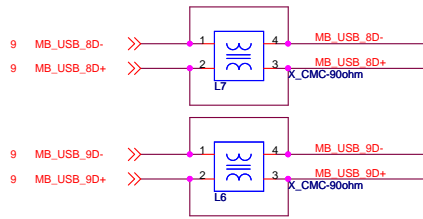
**USB MODE**



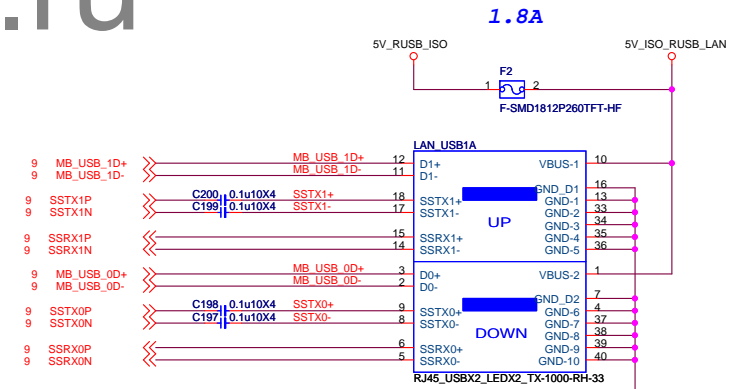
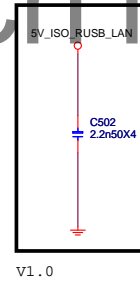
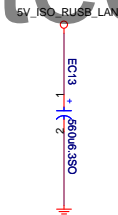
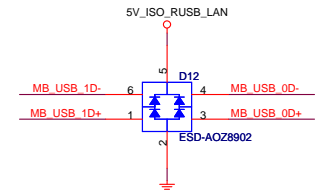
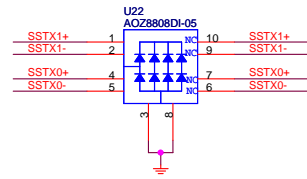
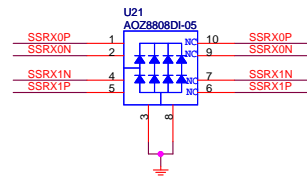
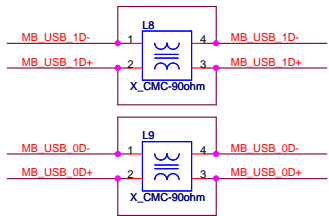
MS-7918

Size Custom	Document Description <b>Rear I/O PS2/USB2</b>	Rev 1.0
Date: Friday, March 14, 2014		Sheet 24 of 53

## Dual USB3 Connector

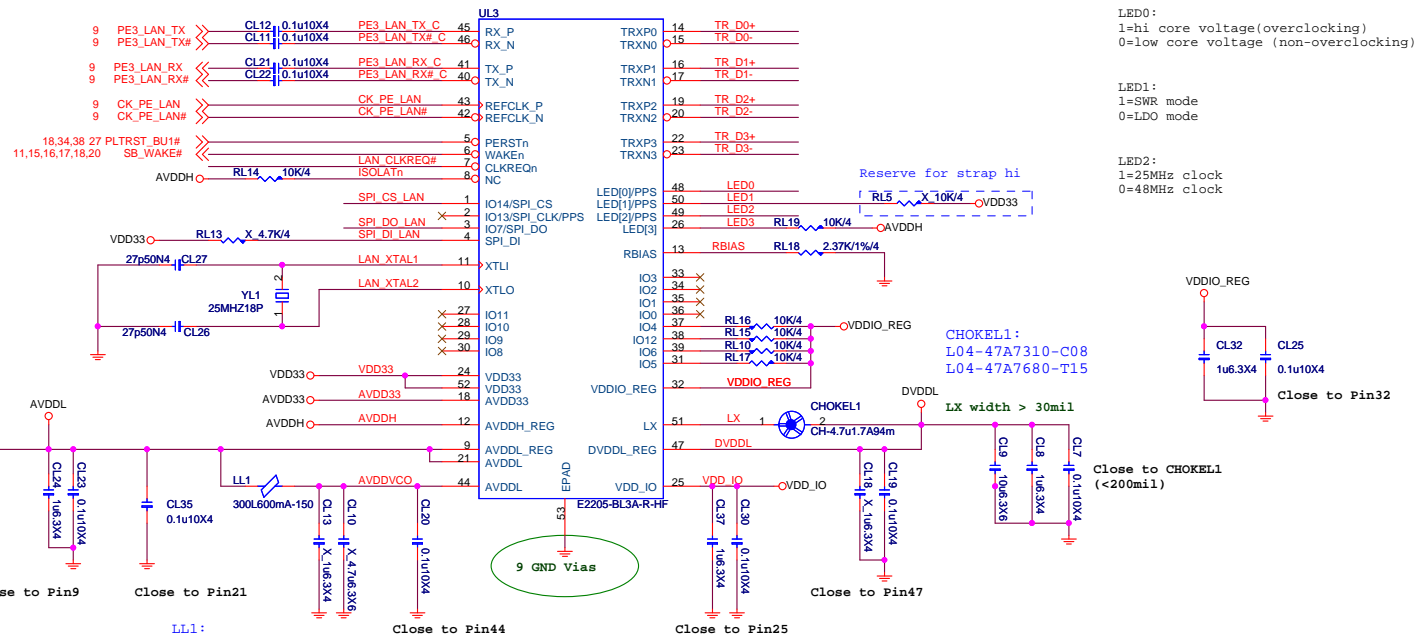
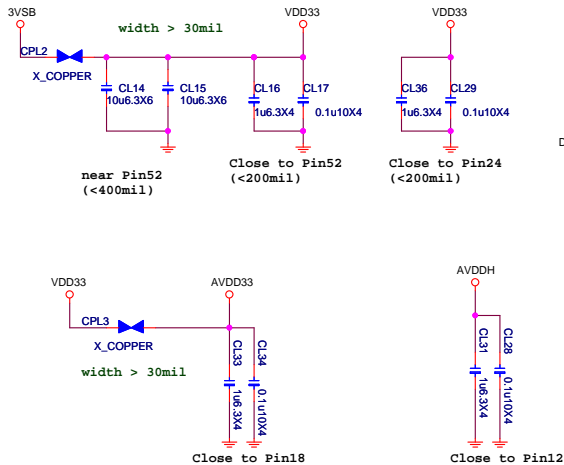
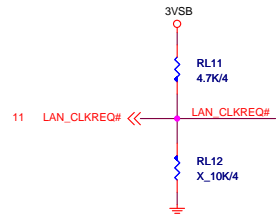


## Dual USB3 Connector (W/ LAN)



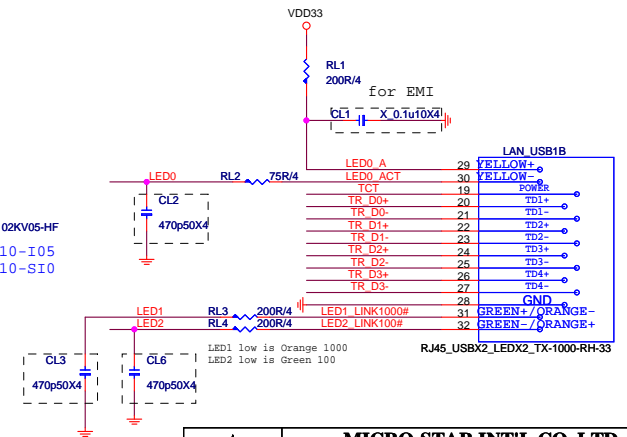
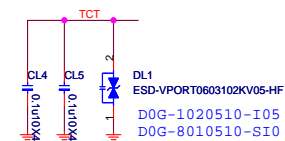
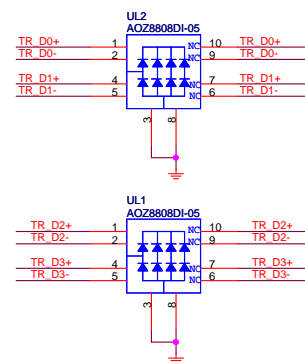
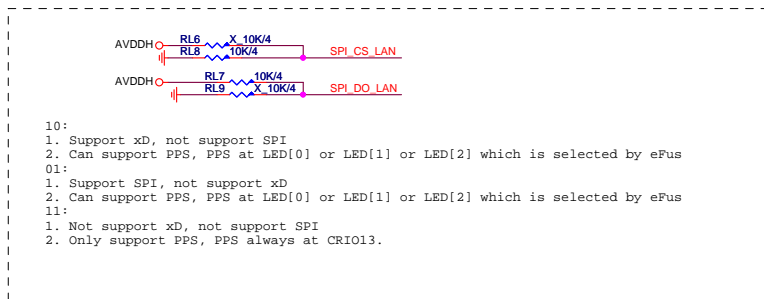


E2205-B Giga LAN



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```
VDD33 power trace should be wider than 30mils;  
AVDD33 power trace should be wider than 30mils;  
VDD_IO power trace should be wider than 30mils;  
VDDIO_REG power trace should be wider than 20mils;  
AVDDH power trace should be wider than 20mils;  
AVDDL power traces should be wider than 20mils.  
DVDDL power traces should be wider than 20mils.
```

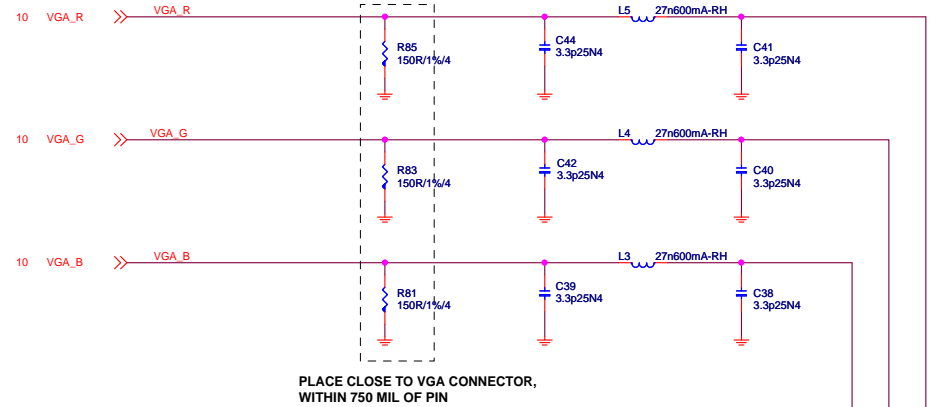
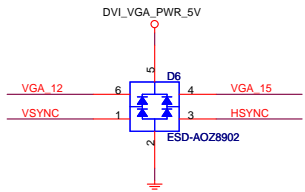
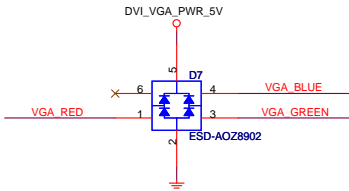
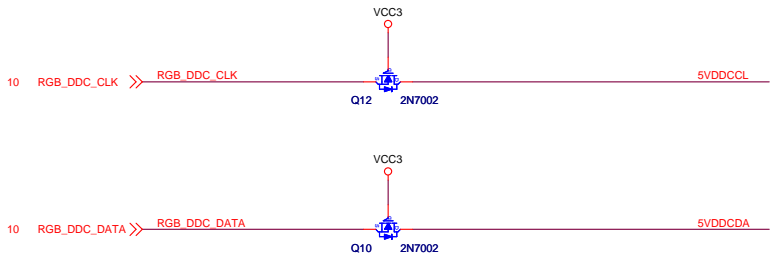
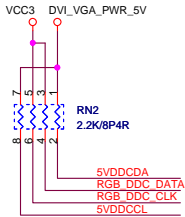


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<b>MS-7918</b>			
Size Custom	Document Description <b>LAN Killer E2205</b>		Rev 1.0
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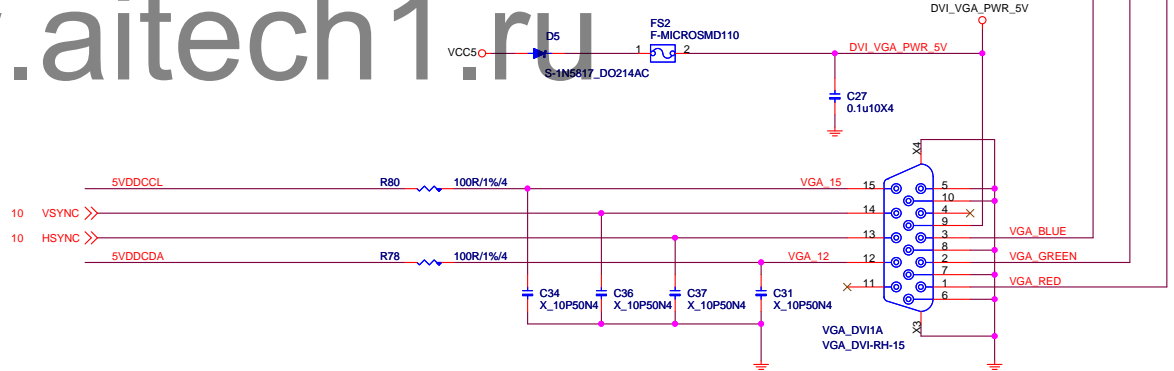
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

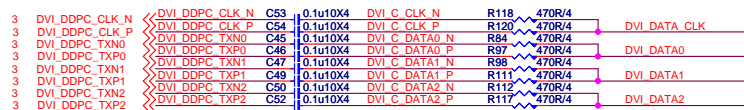
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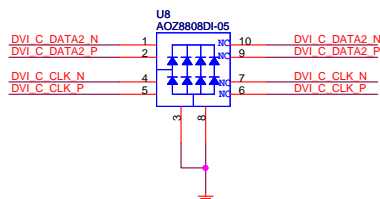
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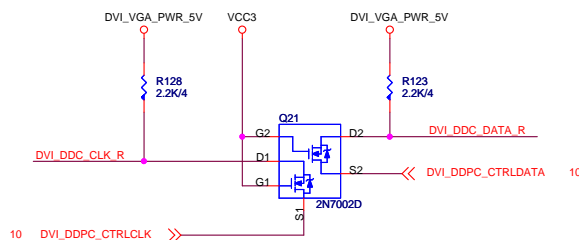
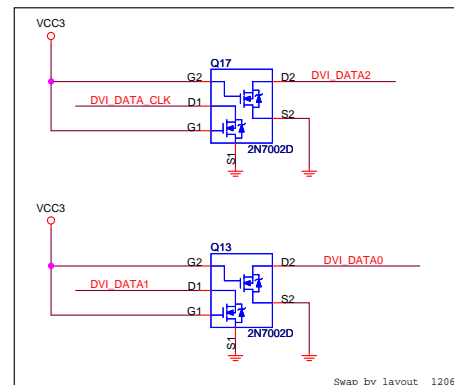
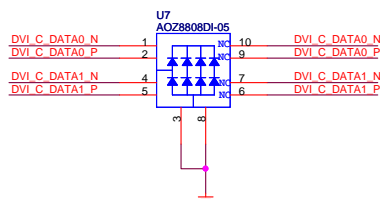
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



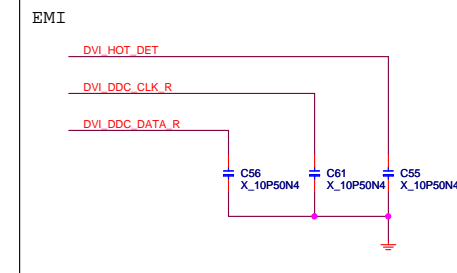
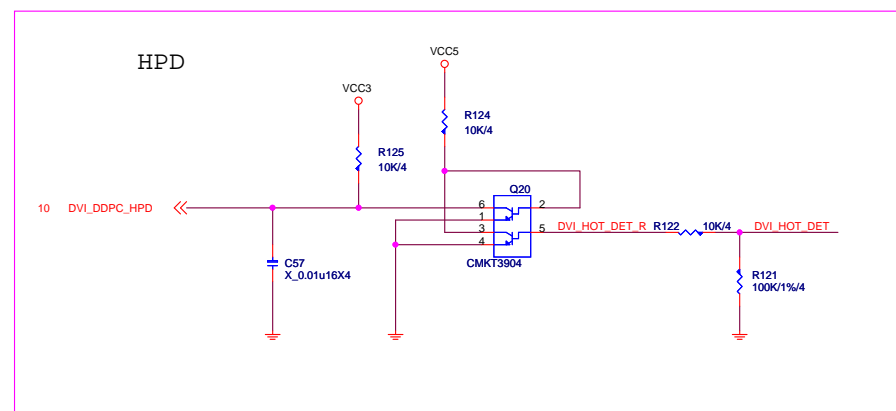
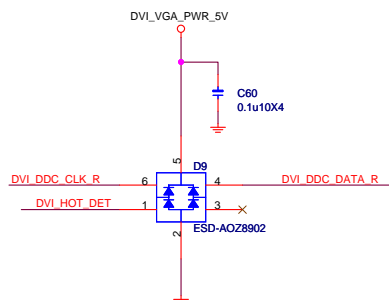
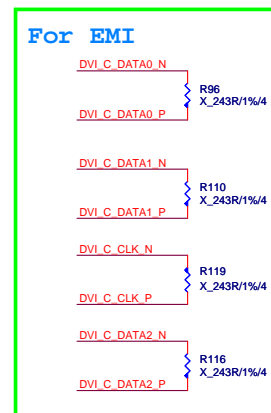
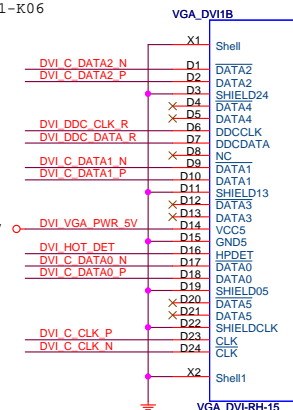
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 D0G-06A050C-A68



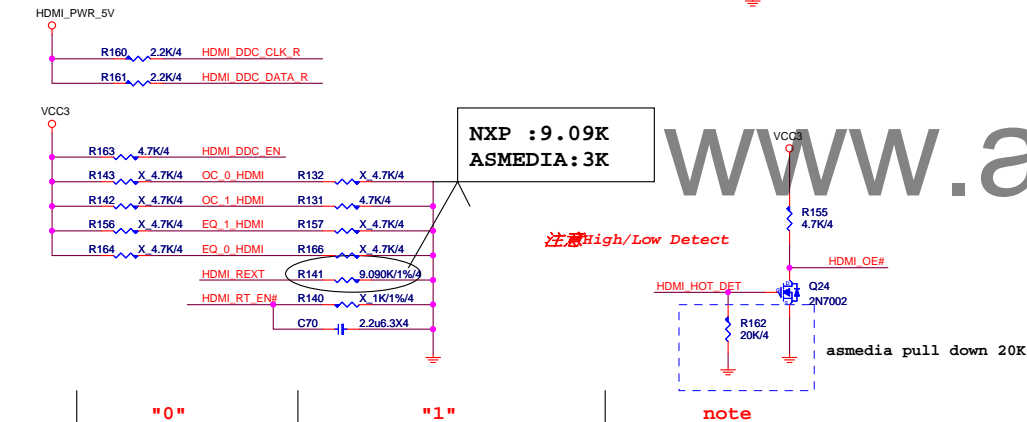
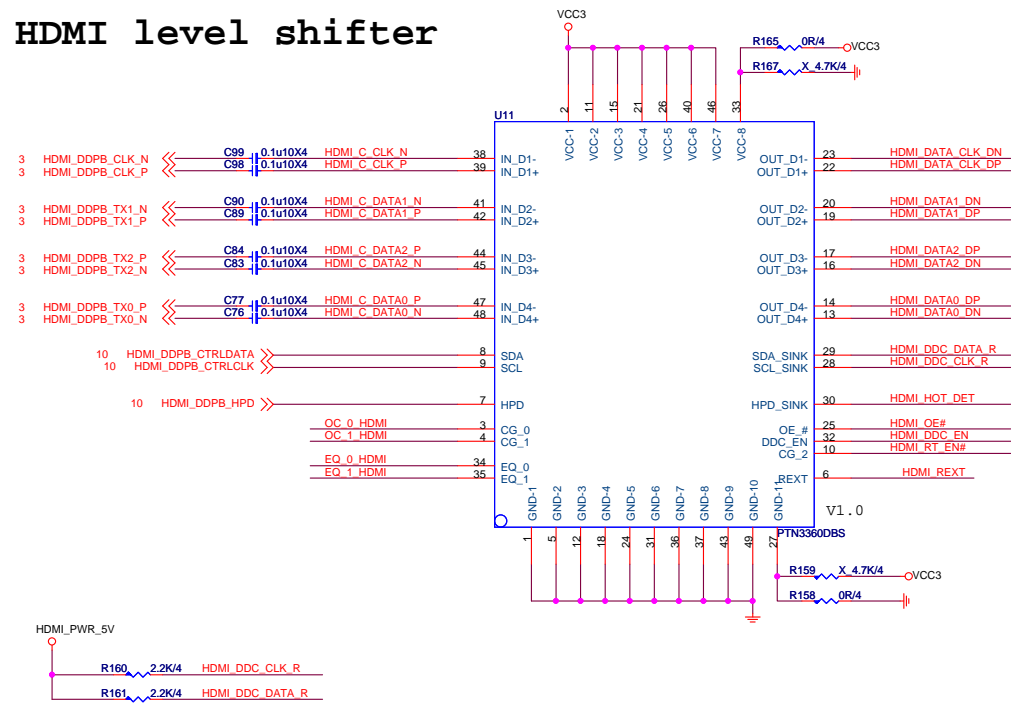
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Check MSI PN  
 N58-39F0231-K06



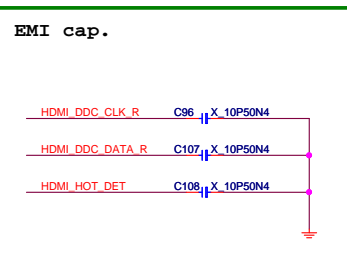
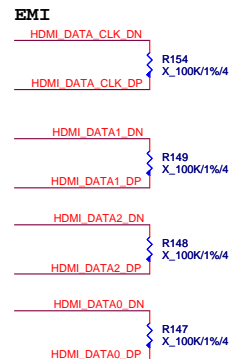
## HDMI level shifter



DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

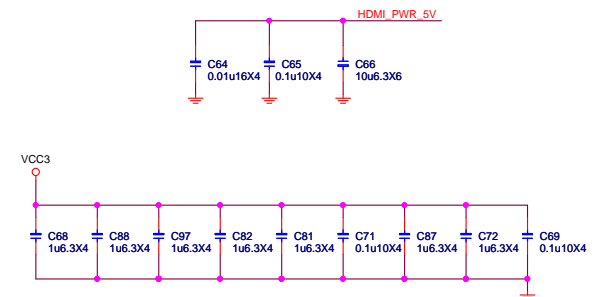
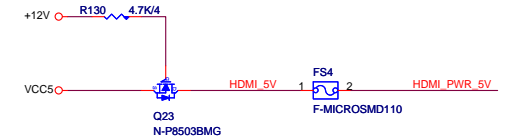
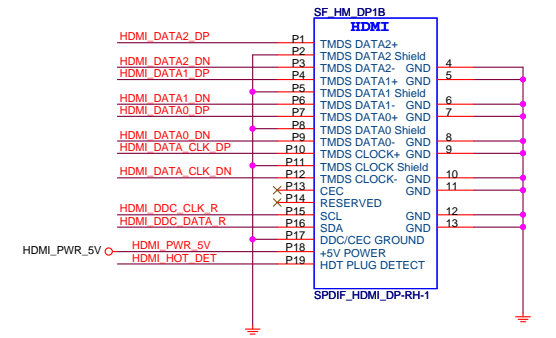
DDC_EN, DDCBUF_EN, OE#	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	



**Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings**

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI_B_CTRL_CLK	HDMI DDC lines for Port B
SDVO_CTRLDATA	HDMI_B_CTRL_DATA		



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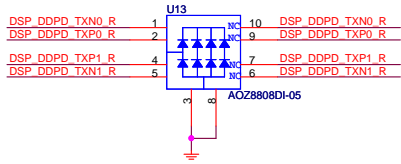
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Document Description  
**HDMI Connector**

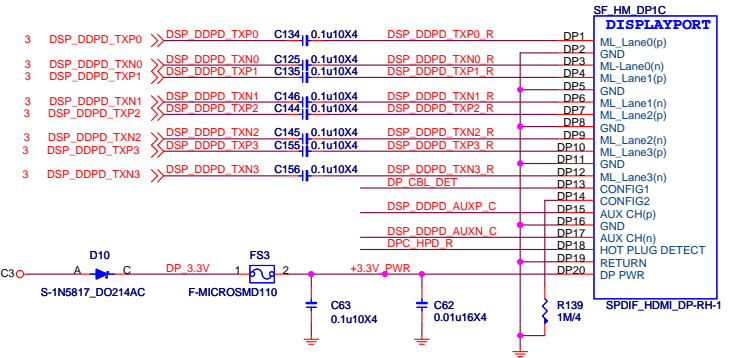
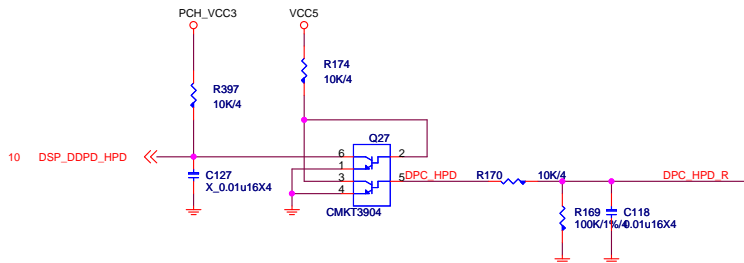
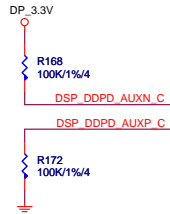
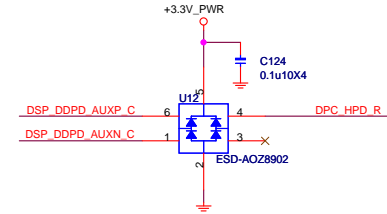
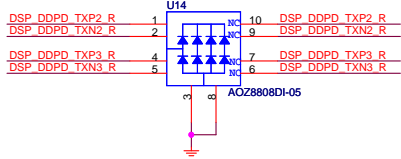
Rev	1.0
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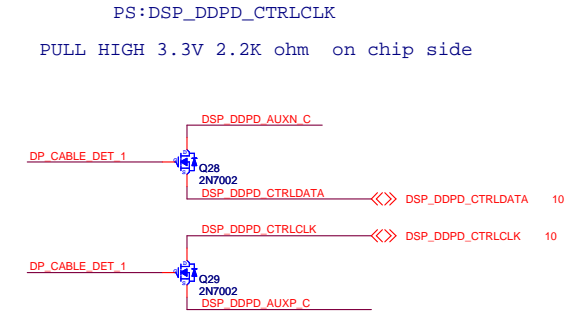
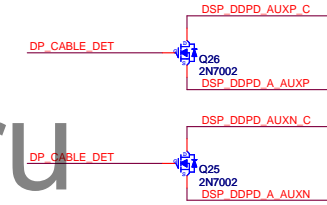


10 DSP\_DDPD\_AUXP >> DSP\_DDPD\_AUXP C136 0.1u10X4 DSP\_DDPD\_A\_AUXP  
10 DSP\_DDPD\_AUXN >> DSP\_DDPD\_AUXN C126 0.1u10X4 DSP\_DDPD\_A\_AUXN



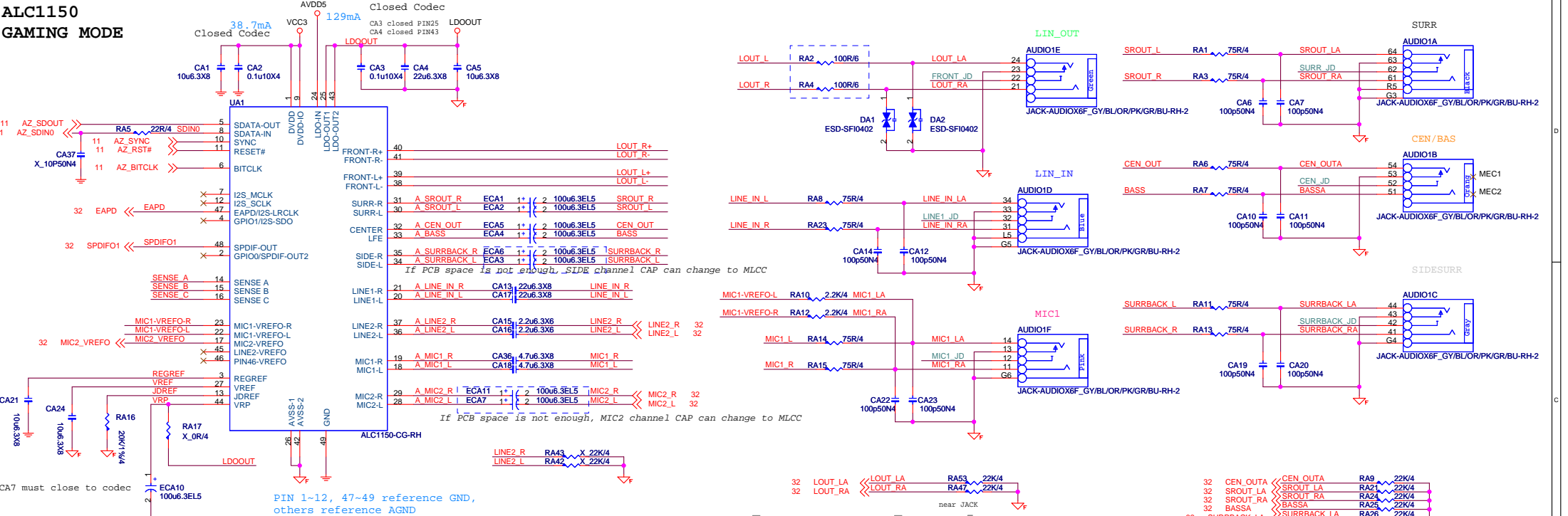
### DisplayPort\*Interoperability Implementation

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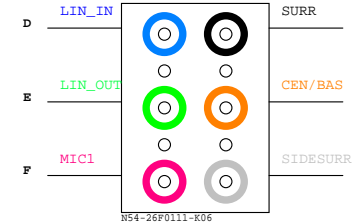
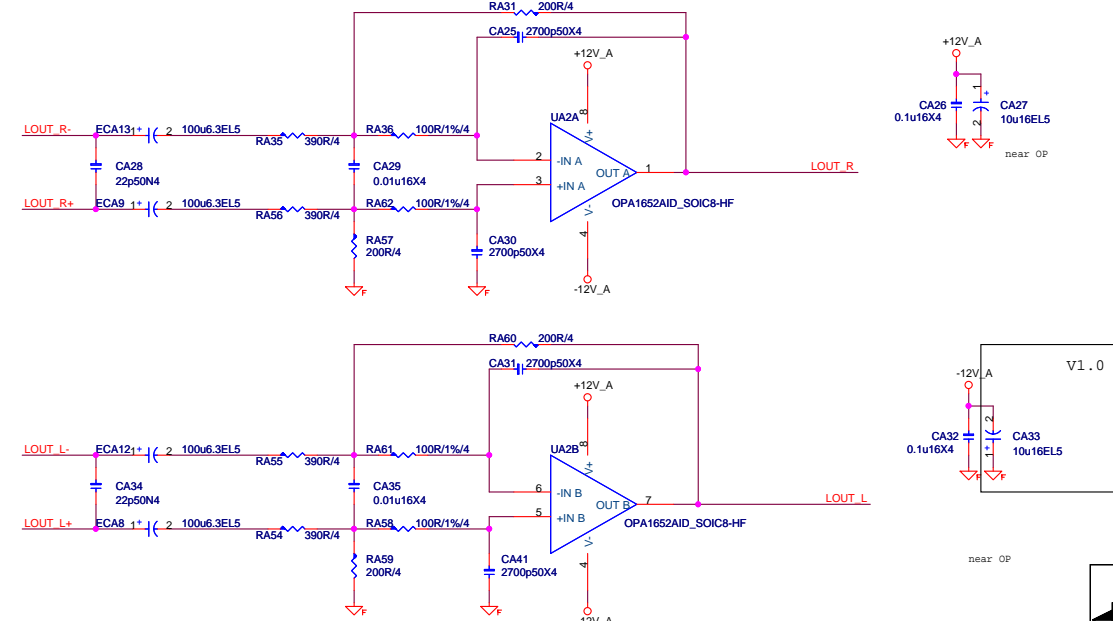
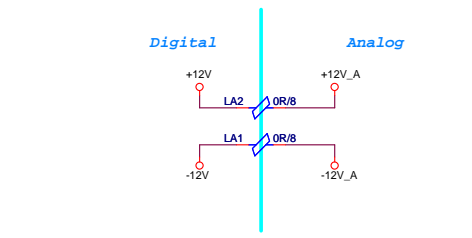
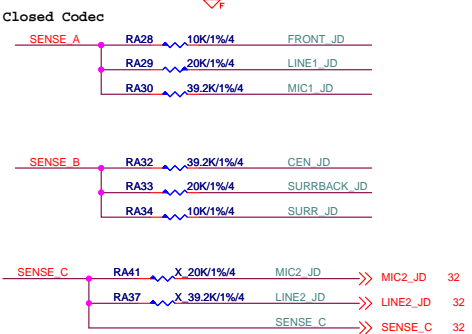


PS:DSP\_DDPD\_CTRLDATA  
PULL HIGH 3.3V 2.2K ohm on chip side

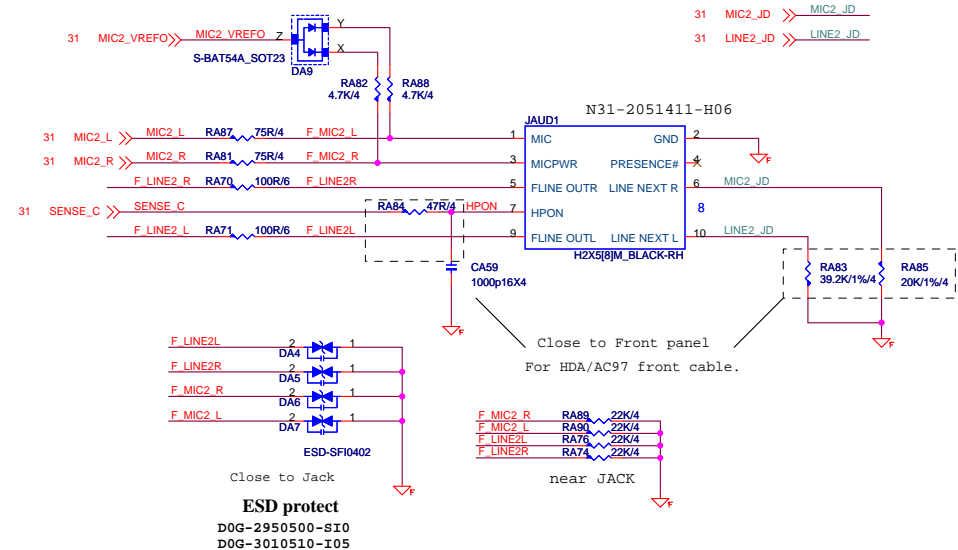
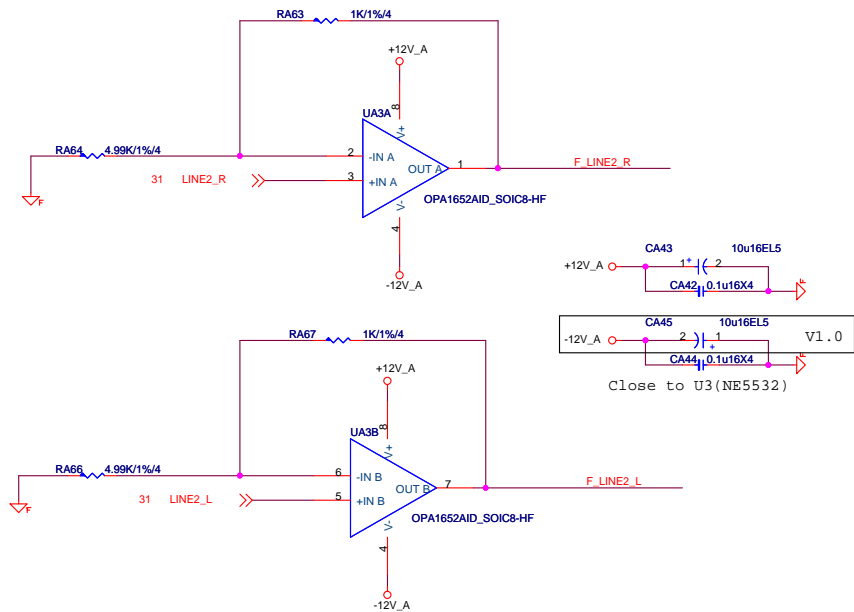
ALC1150  
GAMING MODE



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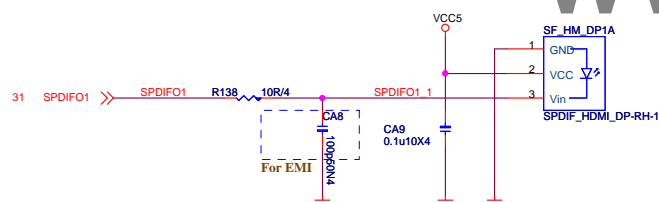






## SPDIF OUT

N58-42M0021-F02 (HDMI+DP+SPDIF)  
N58-06F0201-K06

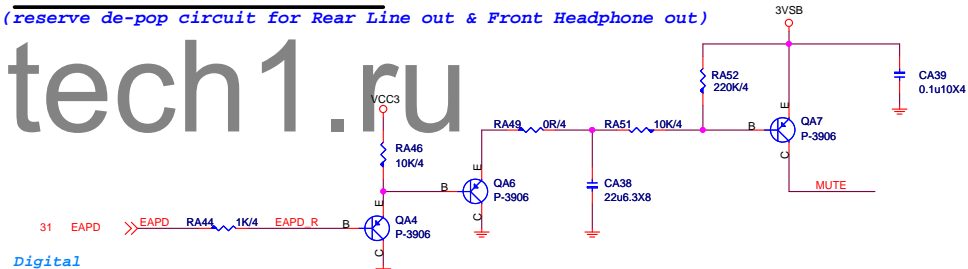


## EMI



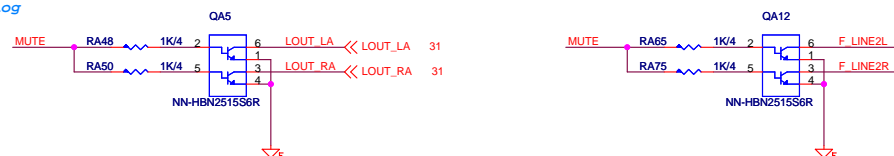
## Rear Line OUT De-POP circuit

(reserve de-pop circuit for Rear Line out & Front Headphone out)

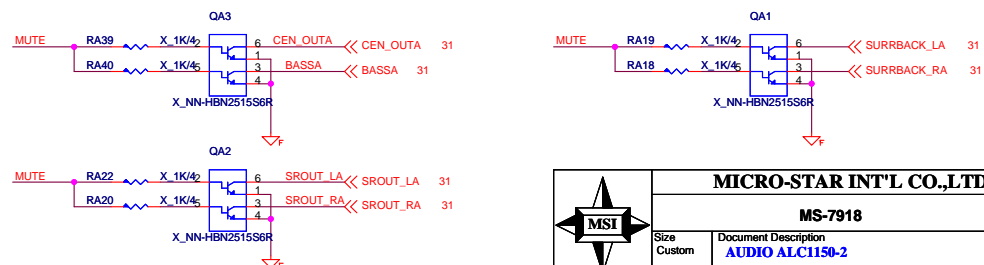


## Digital

## Analog



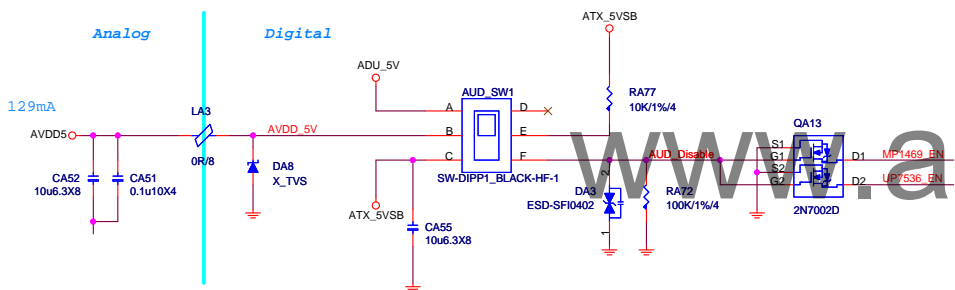
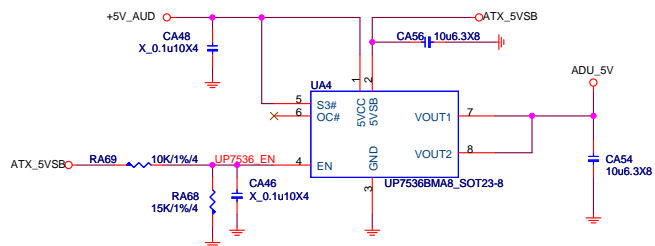
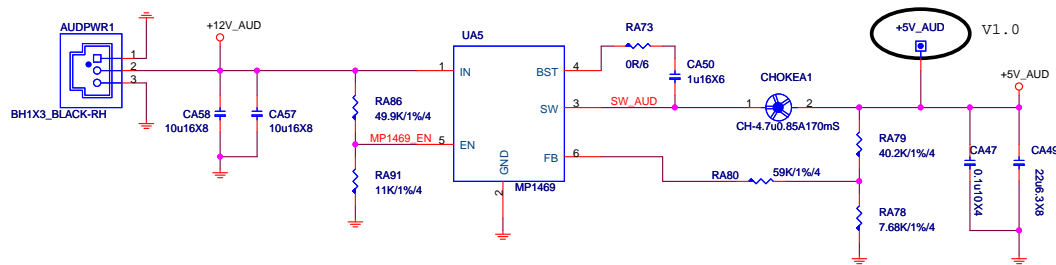
(add de-pop circuit by PM spec or customer request,  
NOTE: add de-pop circuit need to change CA6, CA7, CA12, CA13, CA23, CA24 to TVS)



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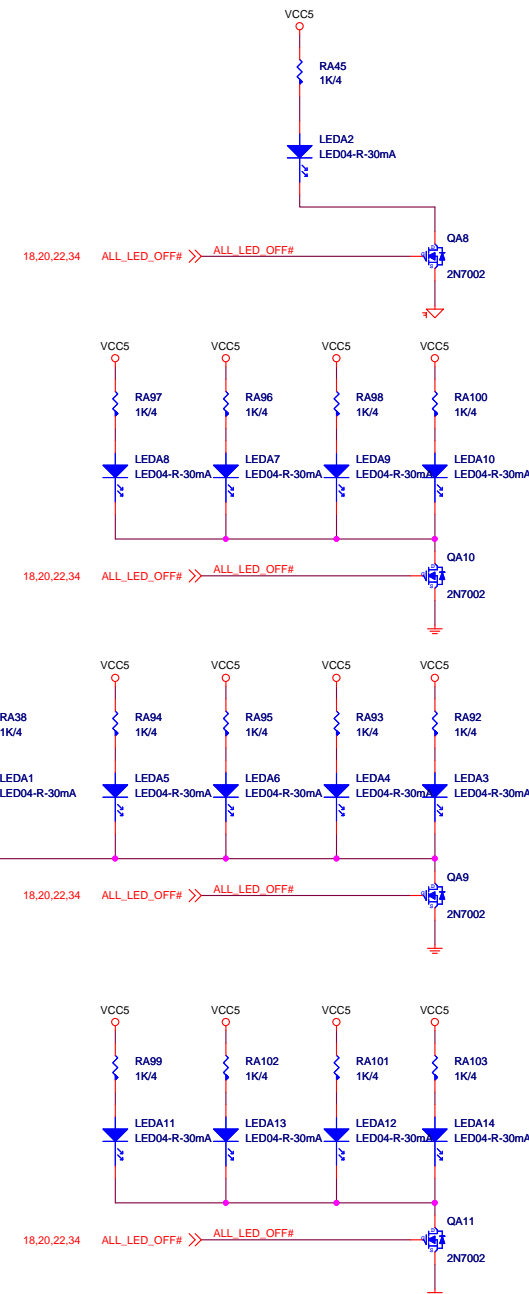


A-B: 5V power from AUDPWR1  
B-C: 5V power from M/B ATX\_5VSB (Default)

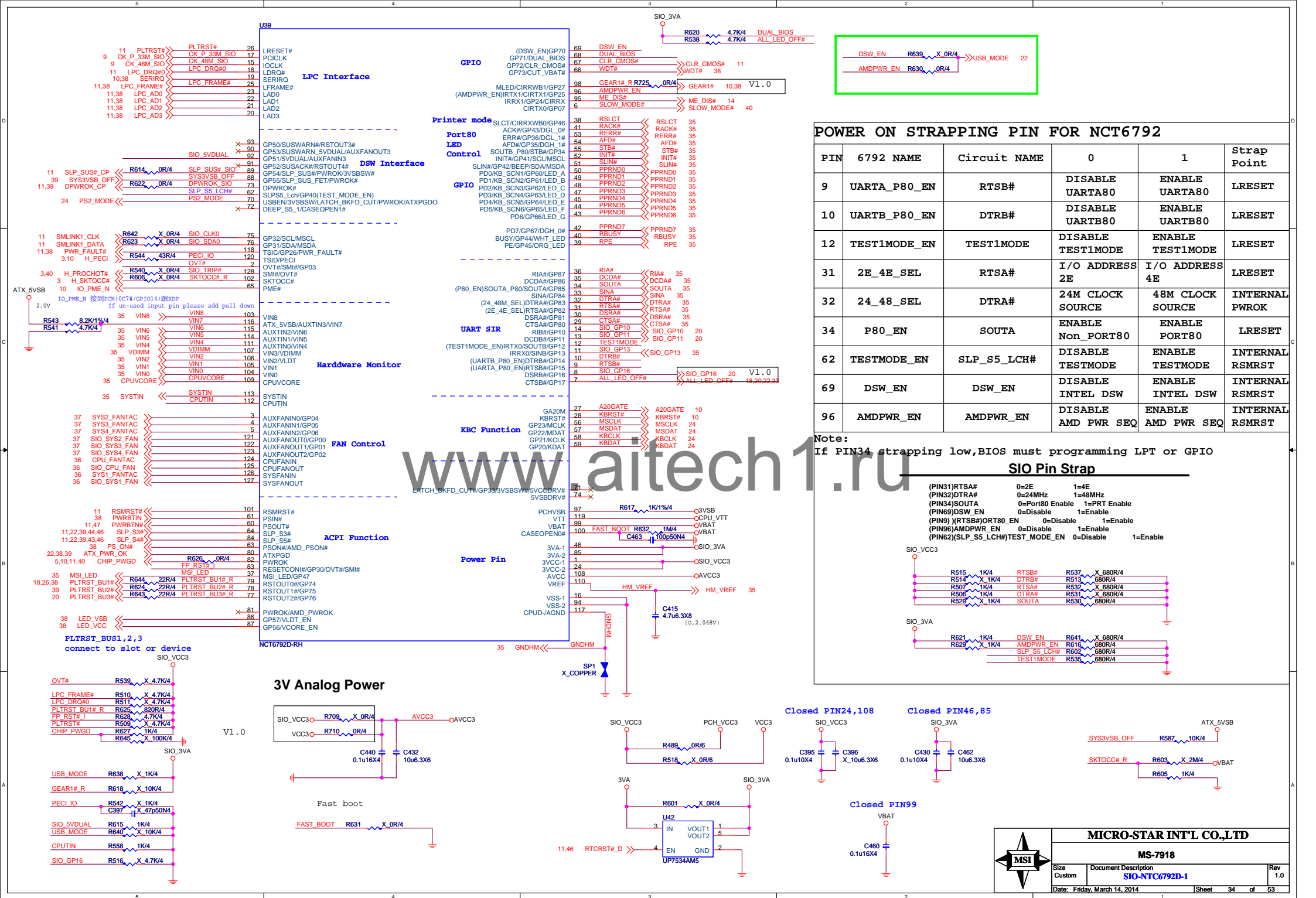
## History:

- 2013/09/25: ALC1150 for Gaming module circuit initial release.
- 2013/10/14: Add audio 5V power switch. Swap MIC1-VREFO-L & MIC1-VREFO-R
- 2013/10/23: Change AUD\_SW1 and to disable external 5V power if switched to M/B ATX\_5VSB.
- 2013/10/29: update AUD\_SW1 P/N.
- 2013/11/01: Change AUDPWR1 to 3PIN

Audio moat is transparent and width 40mil



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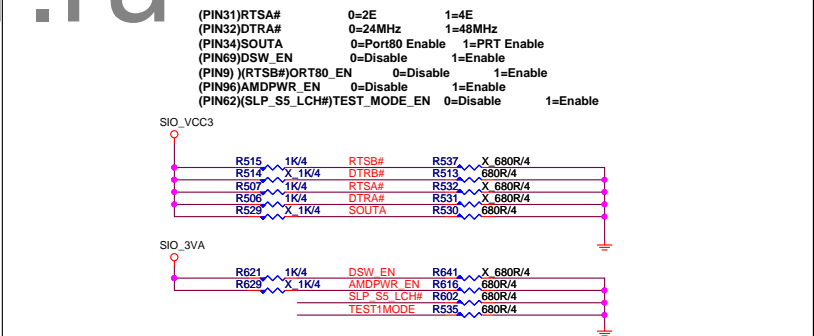


POWER ON STRAPPING PIN FOR NCT6792

PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

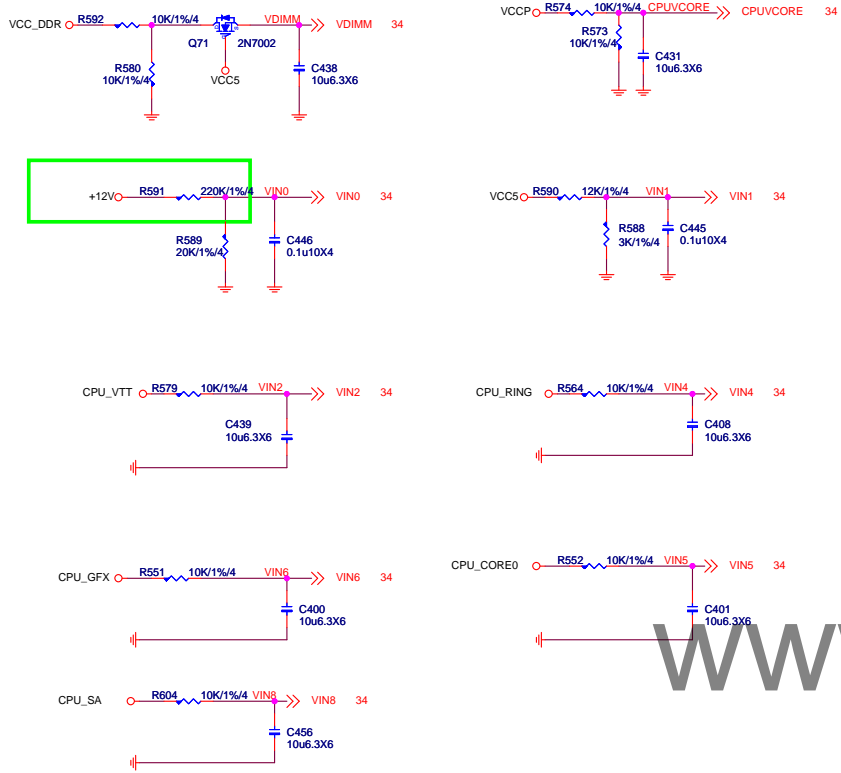
Note:  
If PIN34 strapping low, BIOS must programming LPT or GPIO

SIO Pin Strap

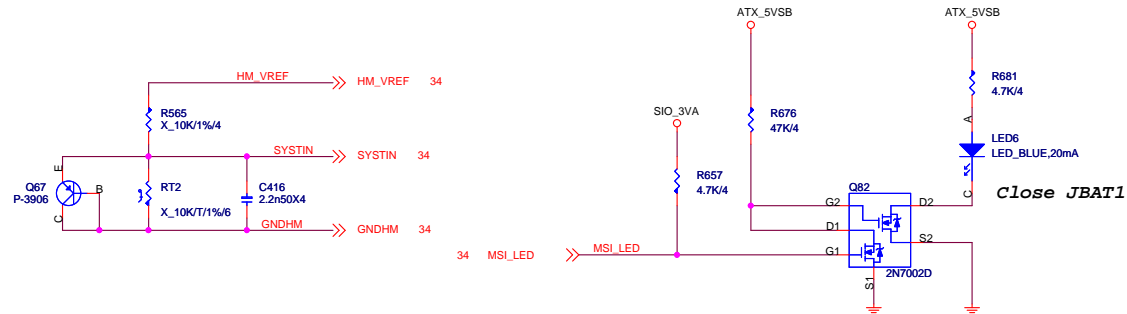


## HW Monitor - Voltage

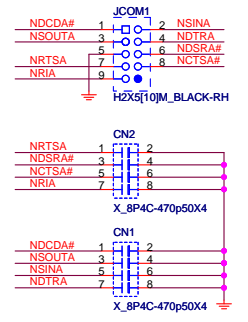
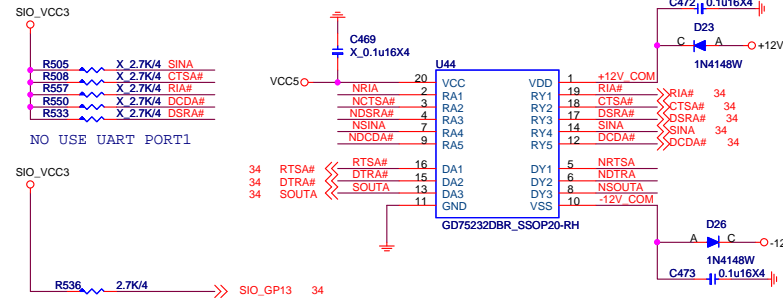
SIO HM Voltage voer 2V will not detect



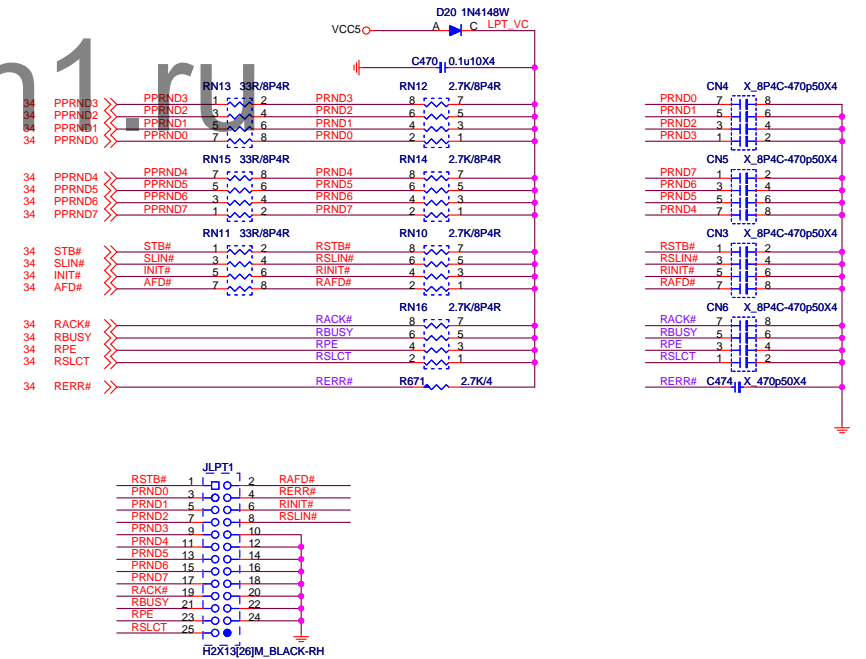
## Thermal Monitor



## SERIAL PORT 1



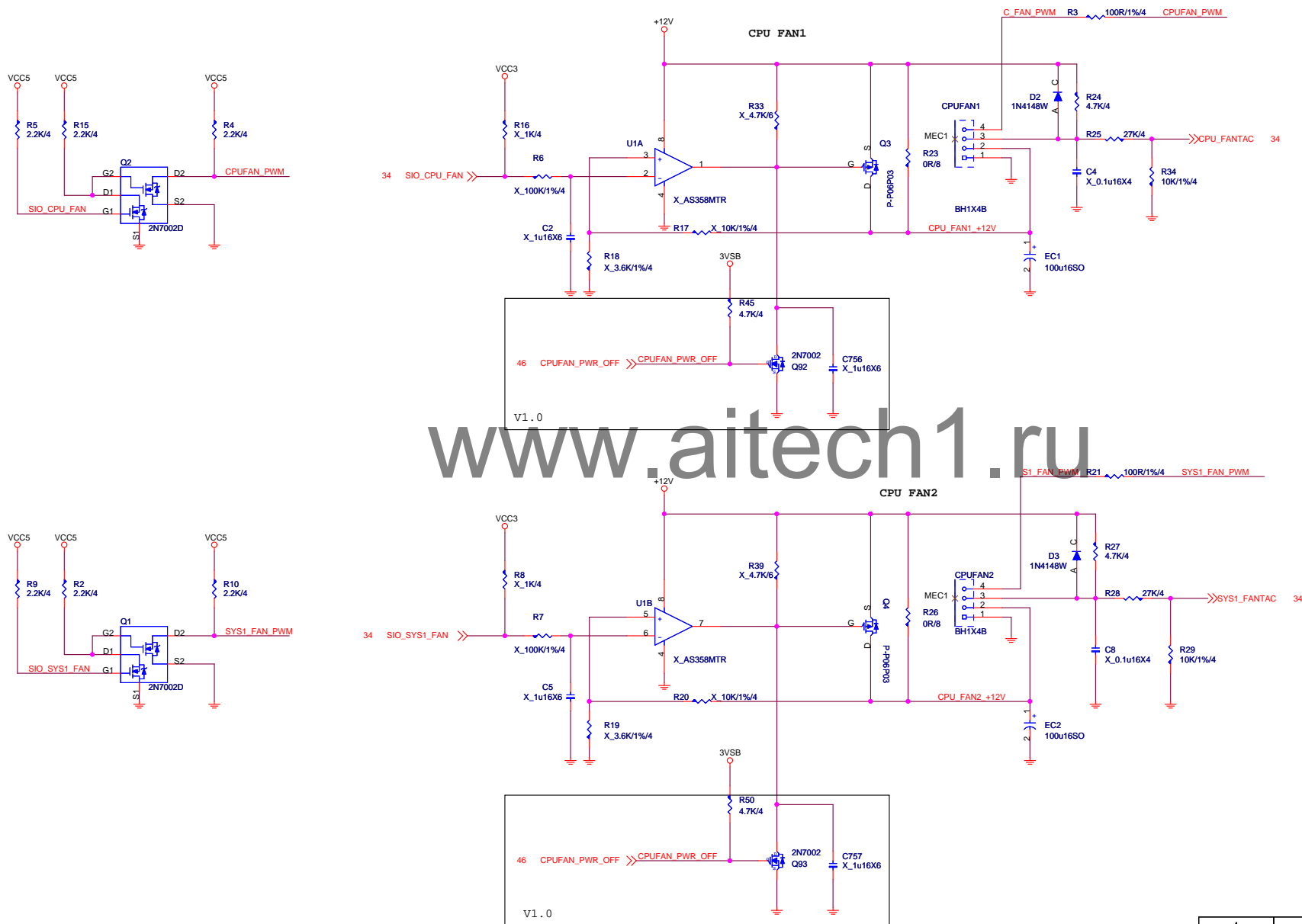
## PARALLAL PORT



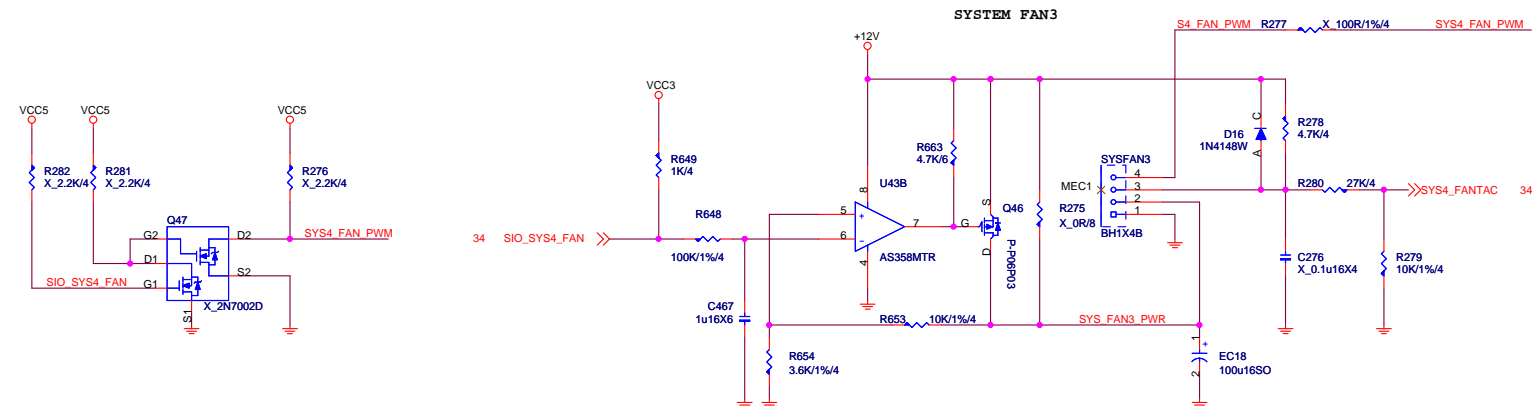
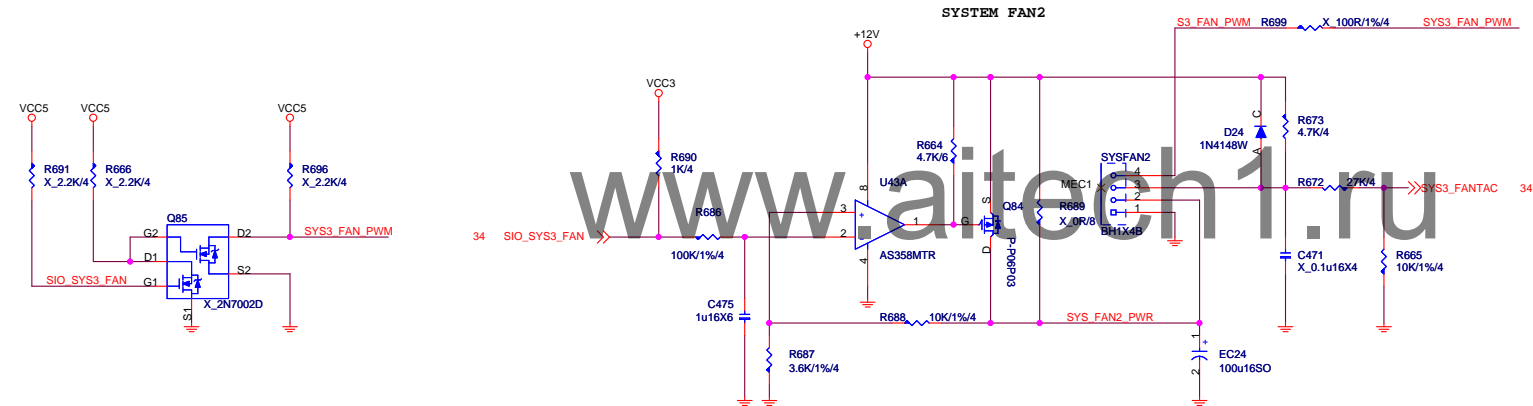
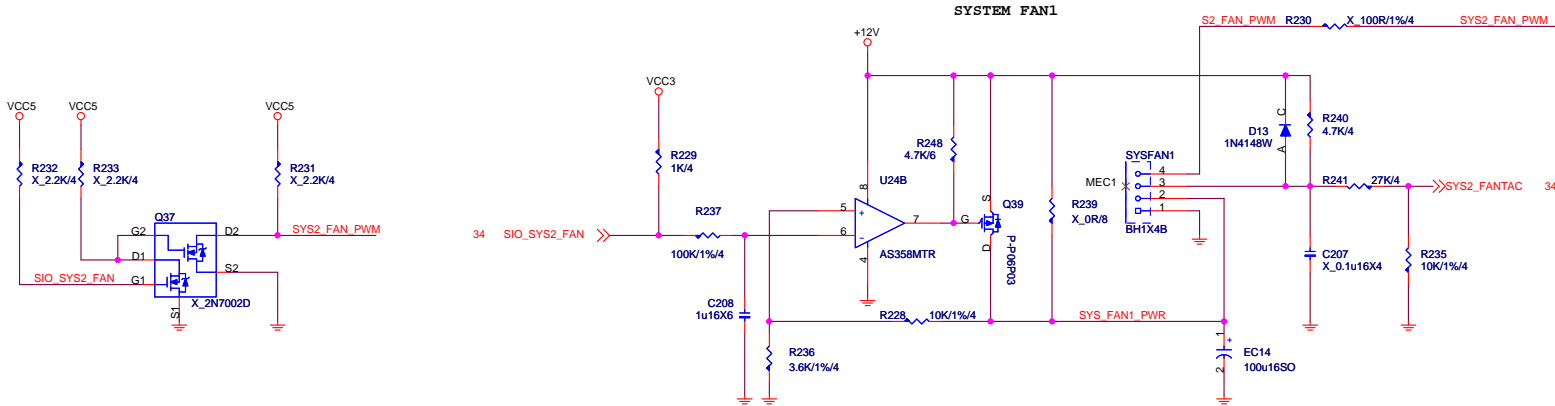
N31-2131151-H06 : 2.0mm  
N31-2131131-H06 : 2.54mm

# Type E : 4 PIN CPU FAN FROM SIO (Smart Fan/PWM MODE )(FOR NCT6776/5533)

## FAN-COUNTROL CIRCUIT



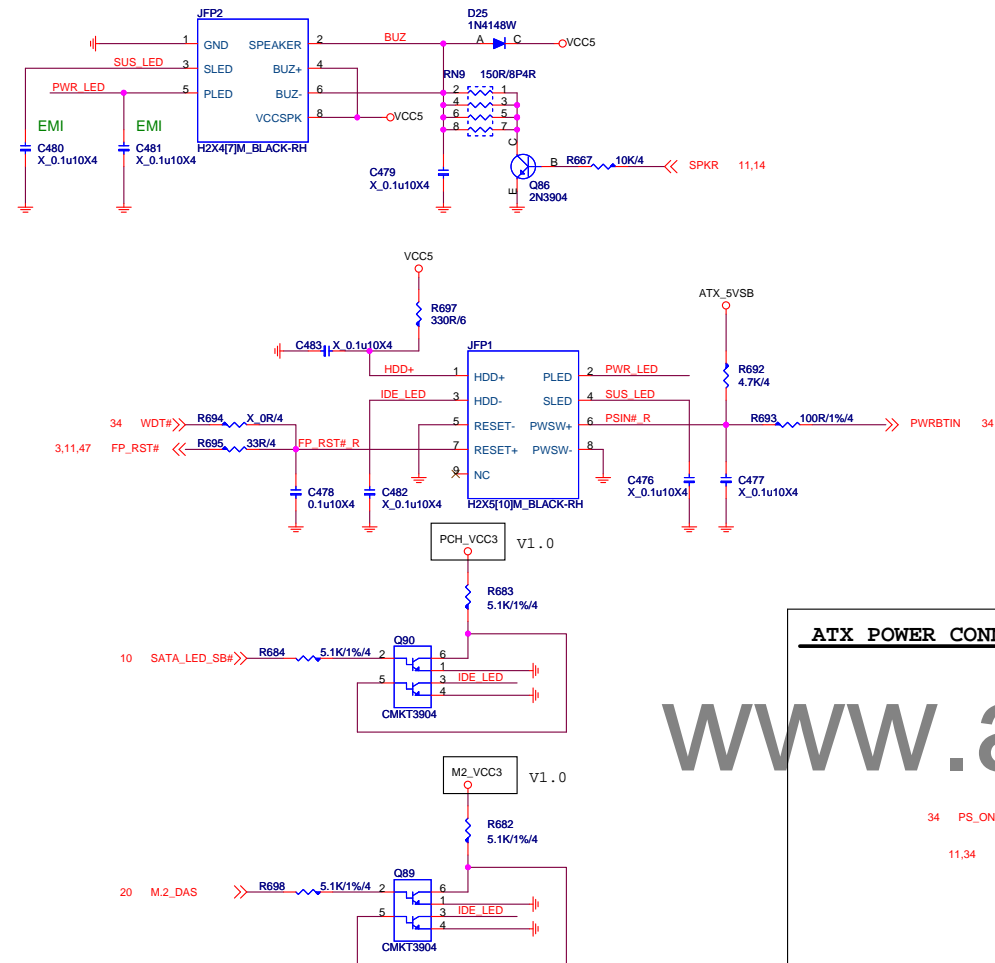
# Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE )(FOR NCT6776/5533)



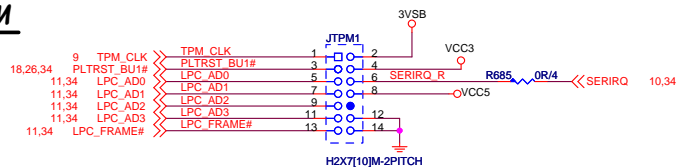
MICRO-STAR INT'L CO.,LTD		
MS-7918		
Size Custom	Document Description SYSTEM FAN	Rev 1.0
Date: Friday, March 14, 2014		Sheet 37 of 53



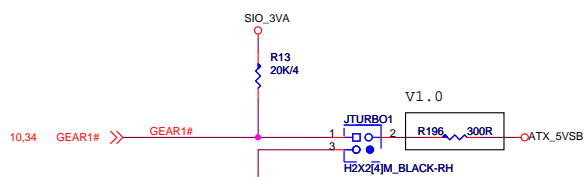
FRONT PANNEL



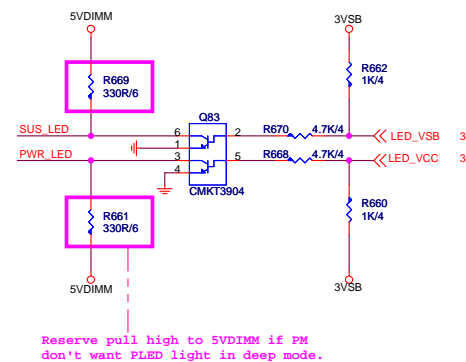
***TPM***



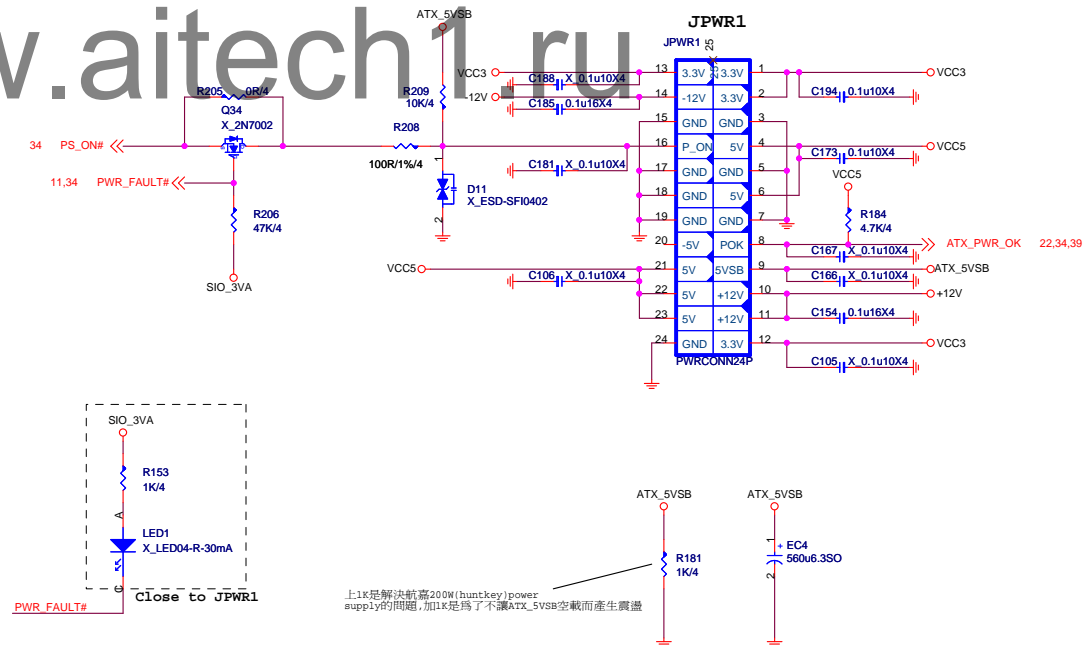
*JTurbo*



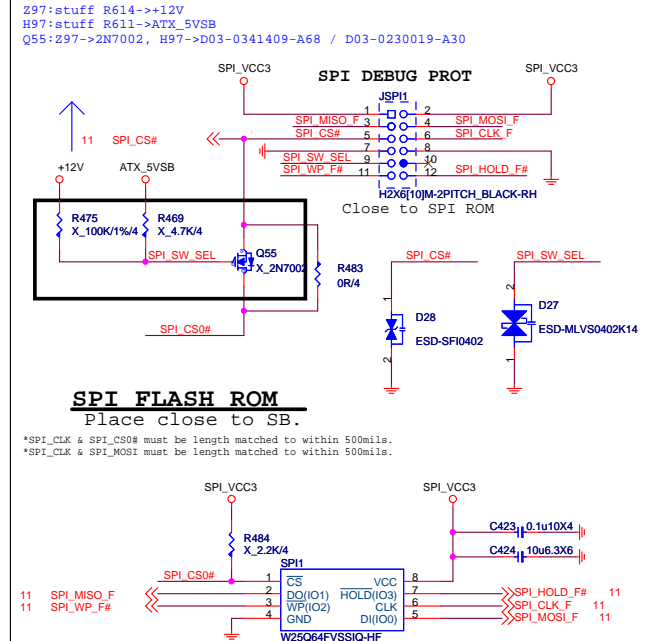
LED ( for Fintek 71869)




## ATX POWER CONNECTOR

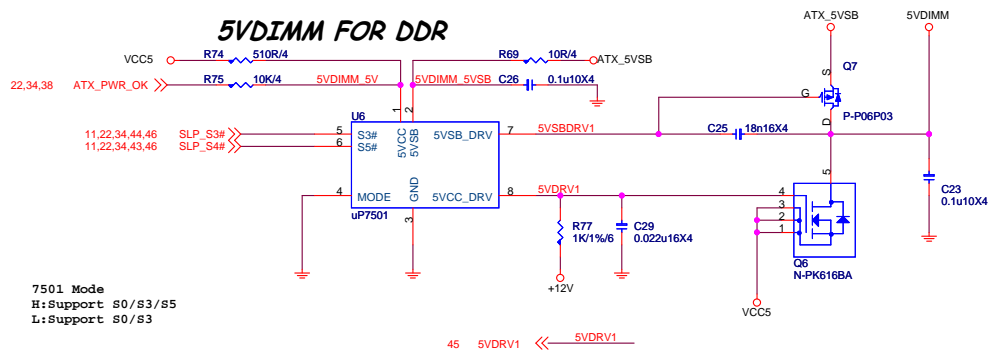


上1K是解決航嘉200W(huntkey)power supply的問題,加1K是爲了不讓ATX\_5VSB空載而產生震盪

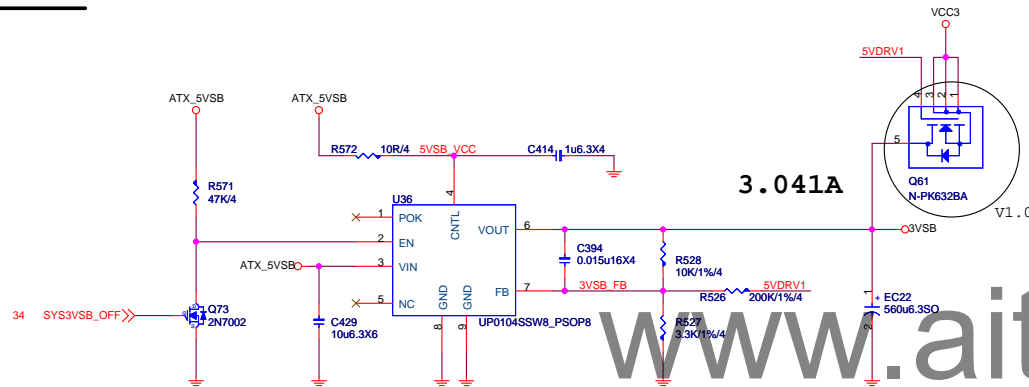


	<b>MICRO-STAR INT'L CO.,LTD</b>		
	<b>MS-7918</b>		
	Size Custom	Document Description <b>ATX F_Panel/TPM</b>	Rev 1.0
	Date: Friday, March 14, 2014		Sheet 38 of 53

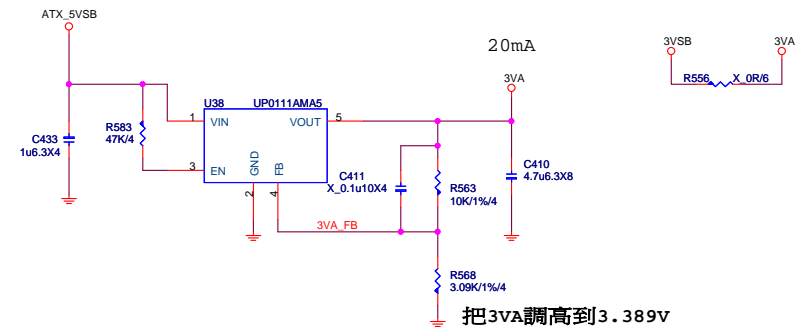
## 5VDDIMM FOR DDR



## 3VSB

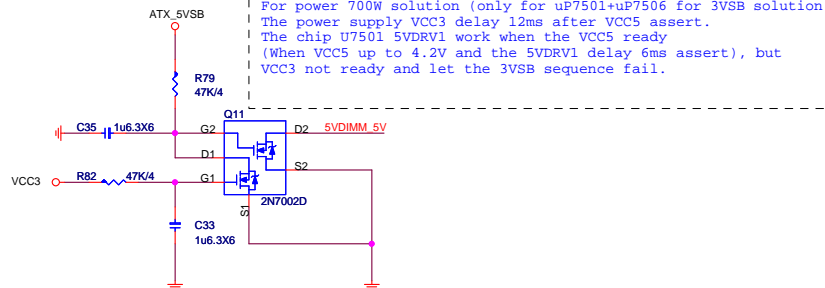
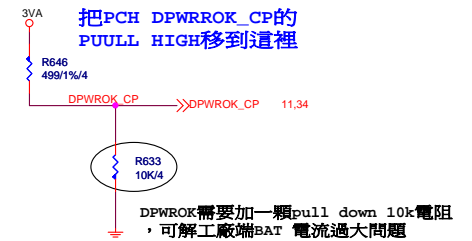


## 3VA



Ver:1.0  
Remove 3VA Power Down circuit

把PCH DPWRROK\_CP的  
PUULL HIGH移到這裡



Remove Buffer Ver:1.0

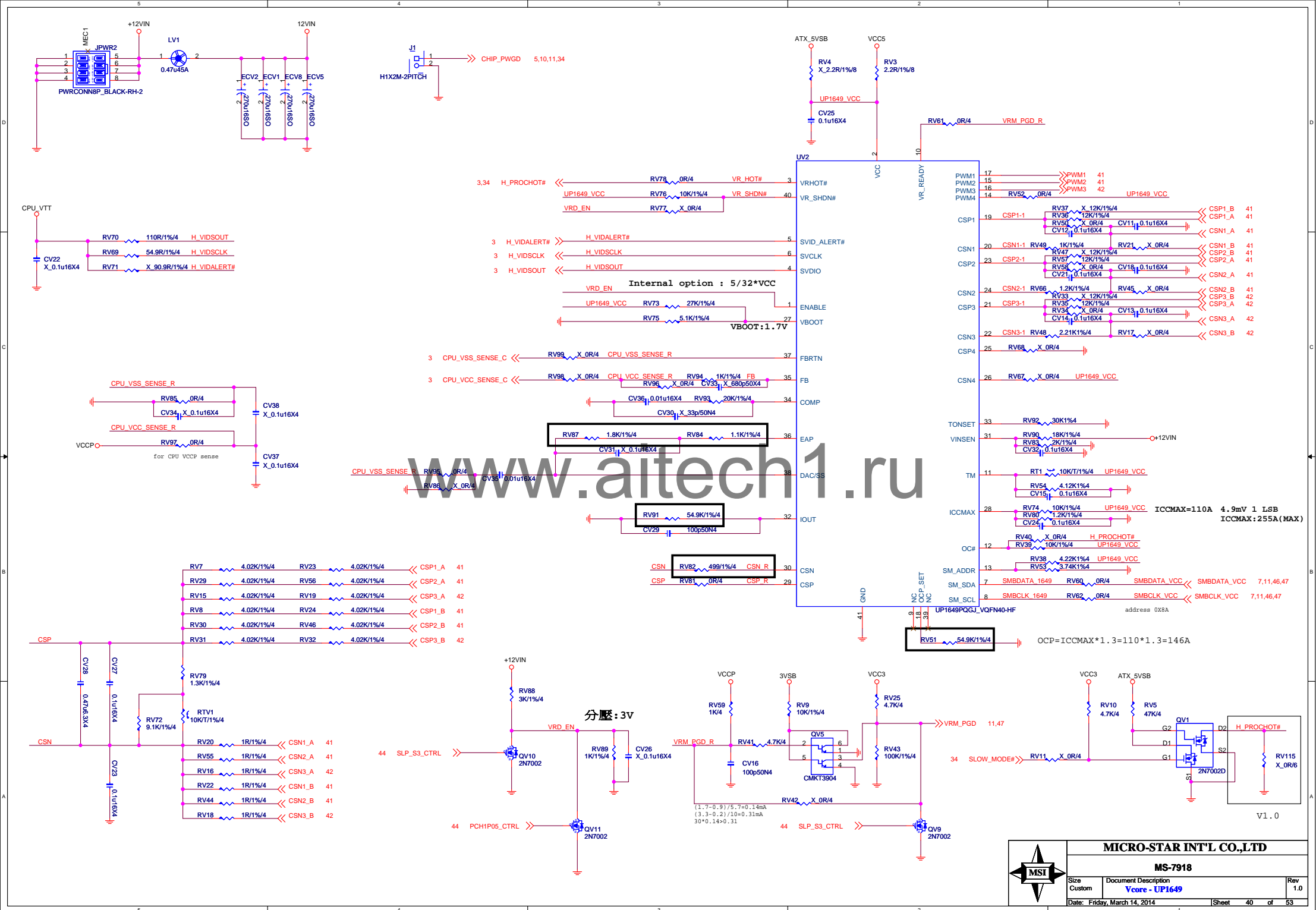
PCIE\_SLOT\_RESET\_N  
from SIO RESET\_BUS2



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Size	Custom
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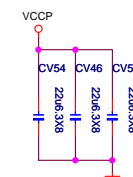
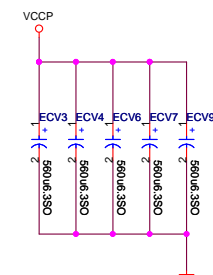
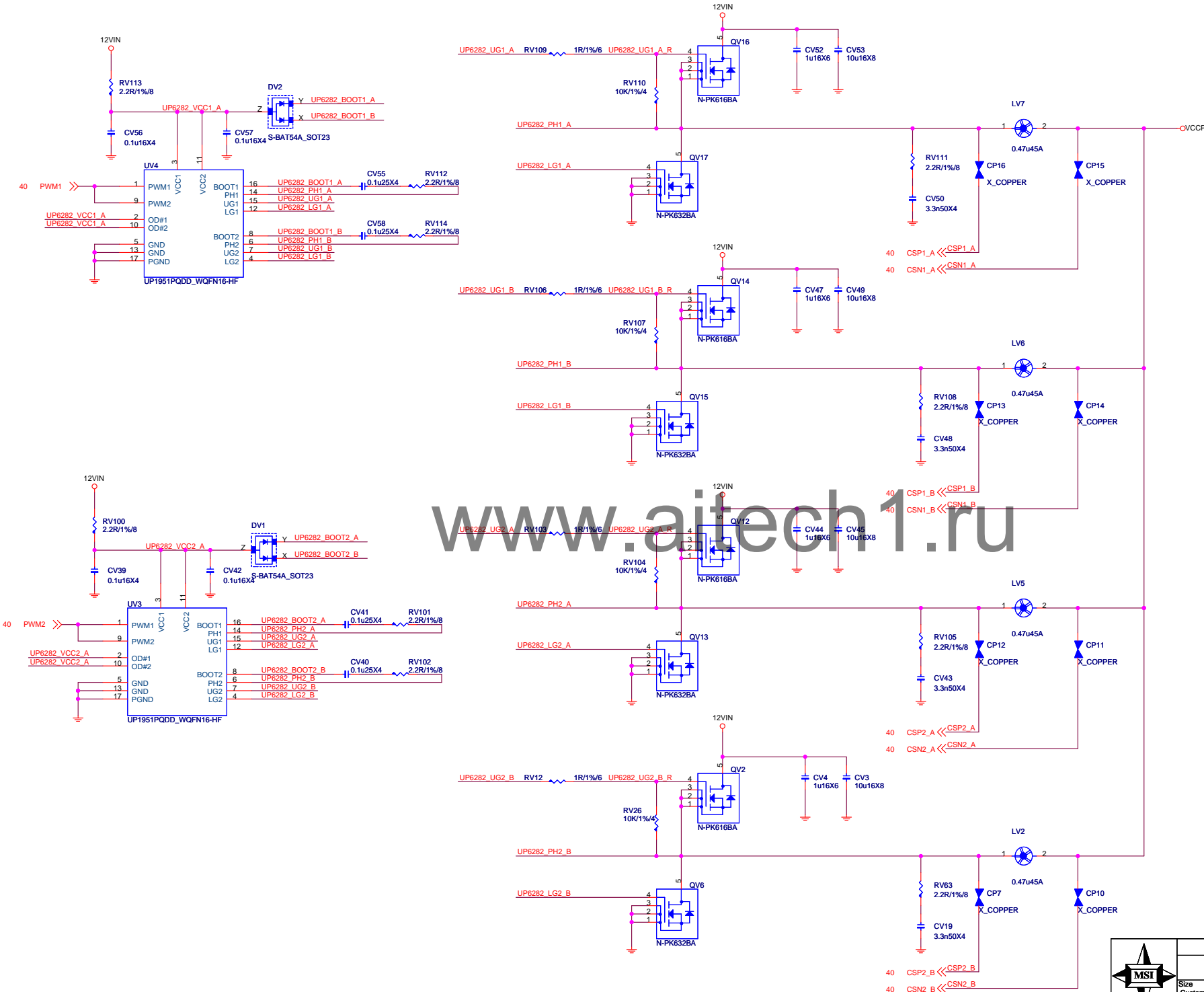
**Document Description**  
**Vcore - UP16**

Rev	1.0
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VCORE 90A TDC:70A  
LL:1.5m ohm



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Custom	UP6282 1-4-Phase	1.0
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# DDR Power:1.5V

DDR3\_1.5V 4.2A+12A+1.115A+6A=23.315A

4.2A FOR CPU

12A FOR 4DIMM

1.115A FOR VTT\_DDR

PCH Core 6A

OCP 23.315A\*1.5=34.9725A

OCP=[20uA\*Rocs(R320)]/4\*Rdson(Low side NXP)2mohm

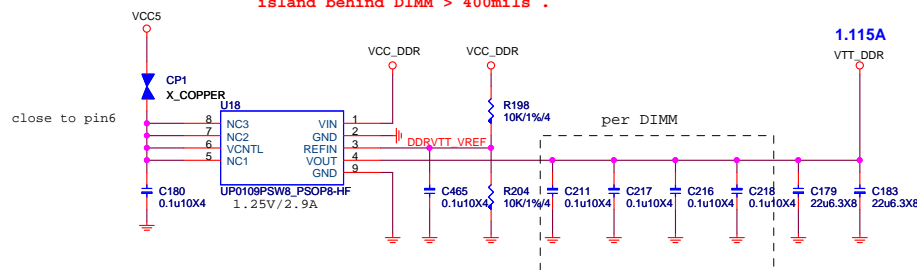
R320=14K ohm

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## DDR VTT Power

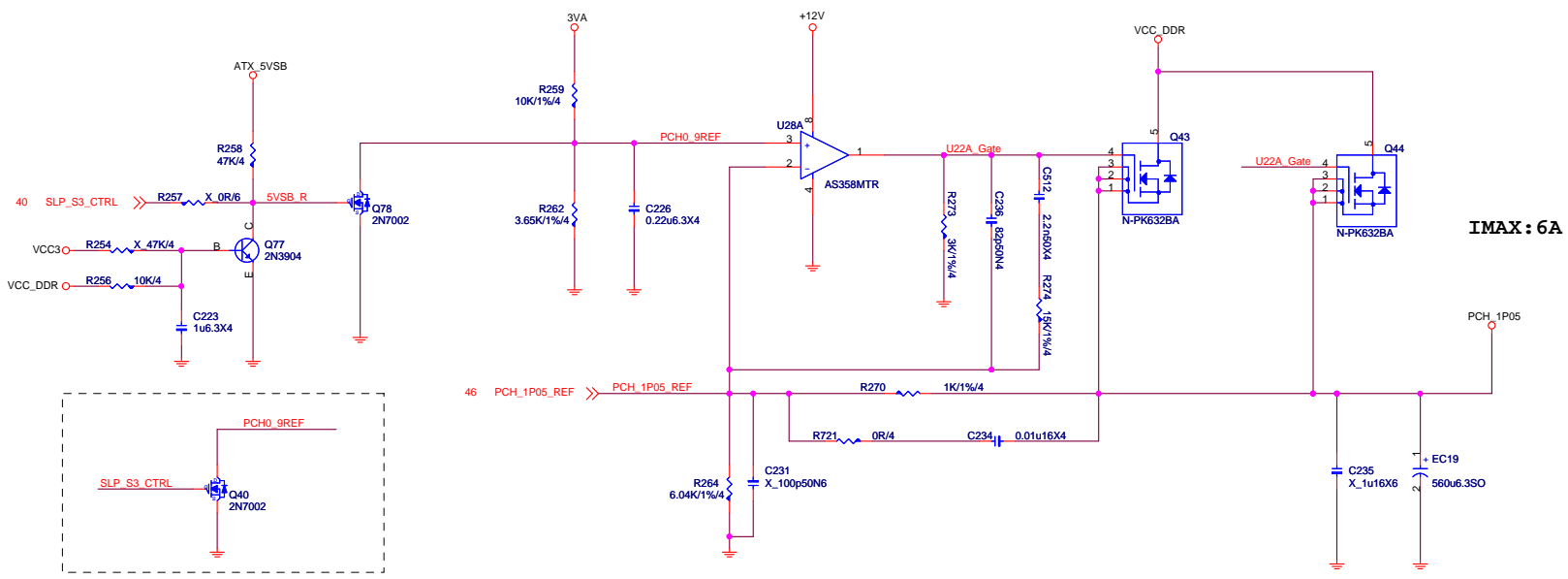
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

P.S. Only for meet Intel power down sequence.

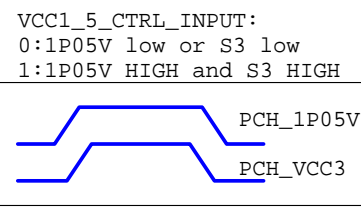
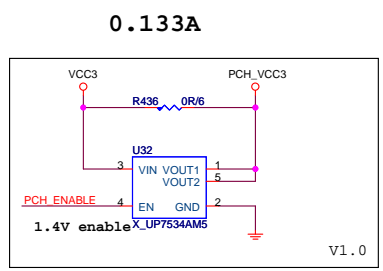


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Custom	DDR POWER - UP1504S	1.0	
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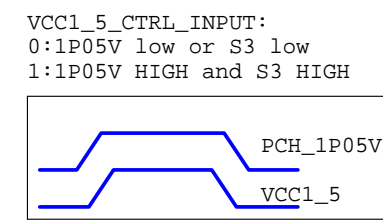
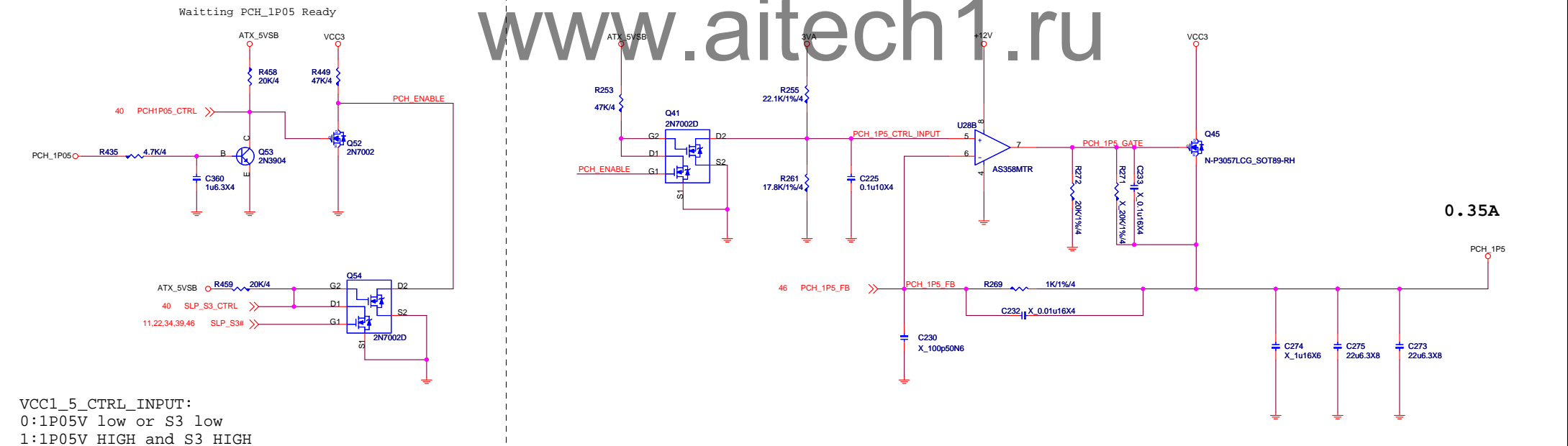
PCH Power:1.05V PCH Core 6A



PCH Power:3.3V



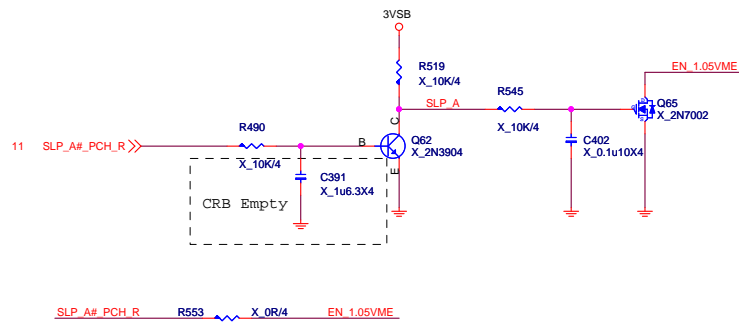
PCH Power:1.5V



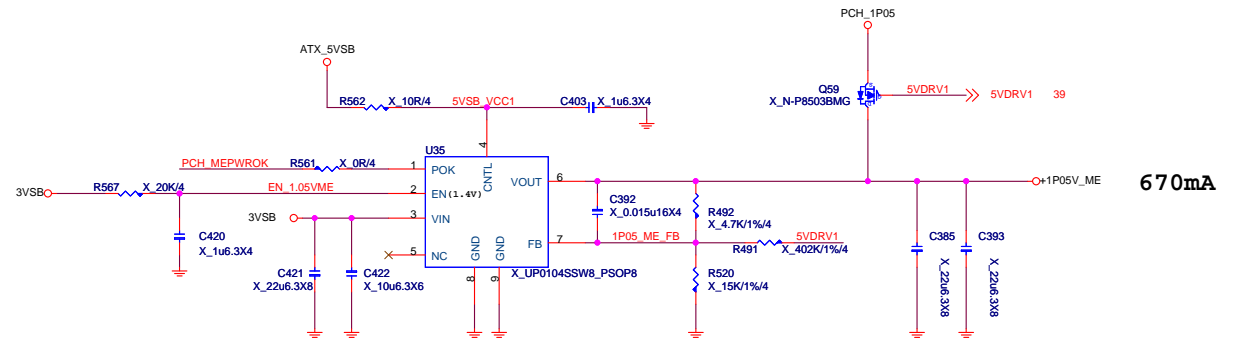


## SLP\_A

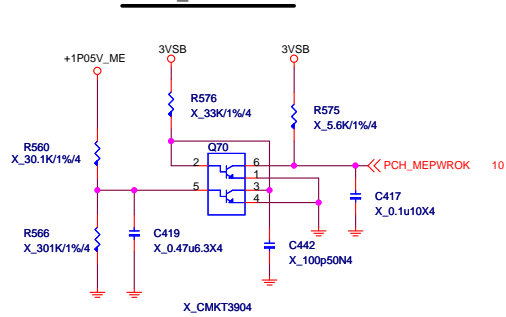
## ME Power Control



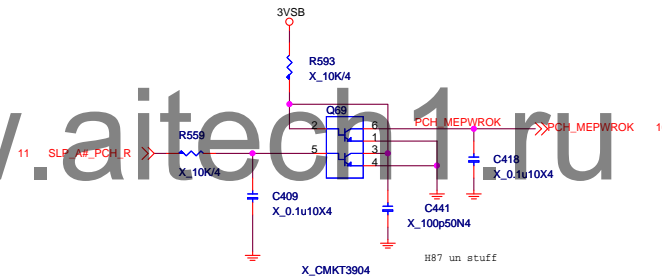
## +1.05V\_ME(VCCIO\_ME)



## PCH\_MEPWROK

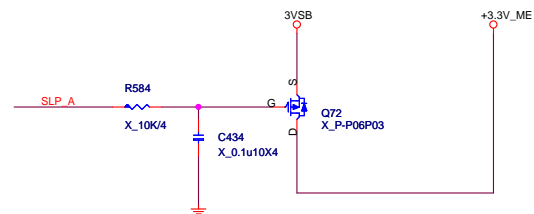


VccASW active to APWROK high 1ms



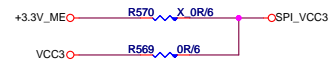
APWROK falling to VccASW falling 40ns

## +3.3V\_ME



For INTEL ME BUG

297->Stuff R569  
H97->Stuff R570

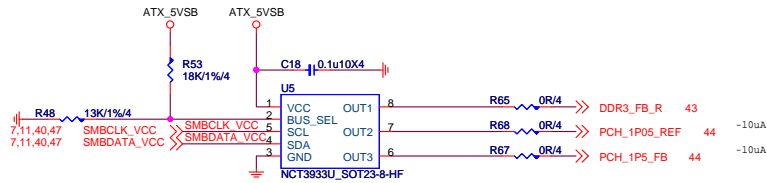


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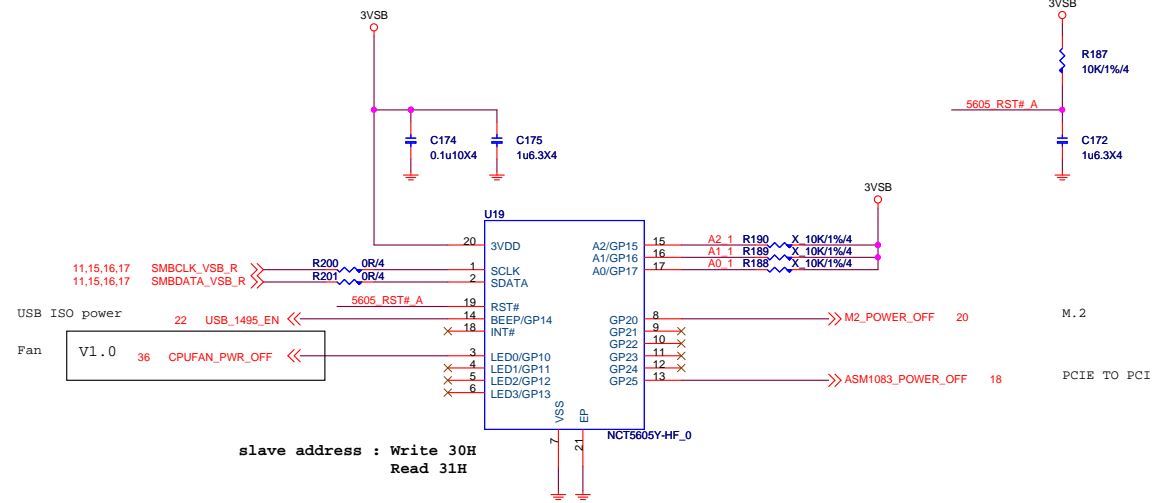
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0x26:RH=18K,RL=13K

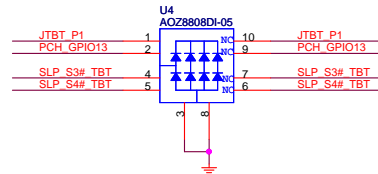
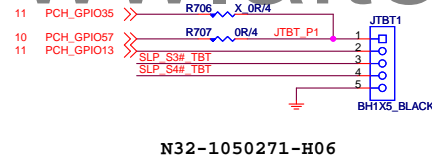
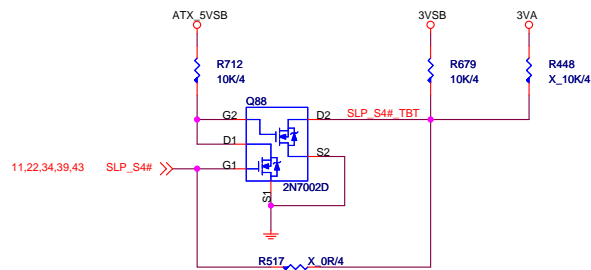
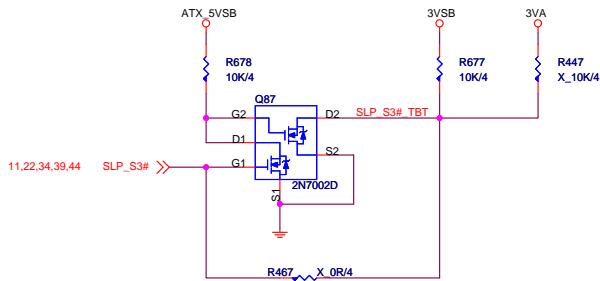


Close TO VCC\_DDR Plan



slave address : Write 30H  
Read 31H

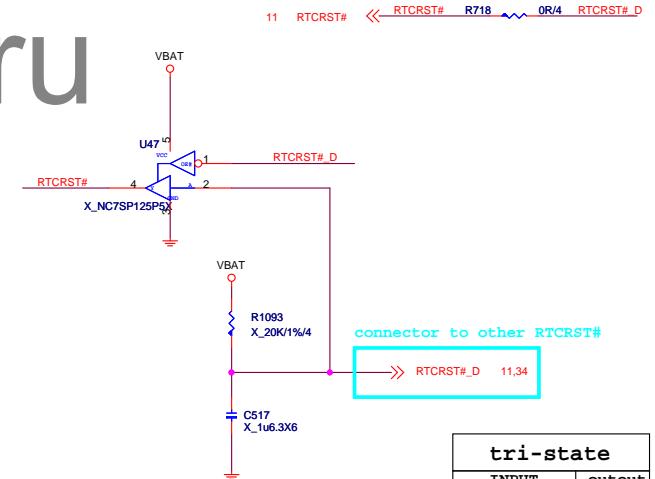
## JTBT



V1.0

V1.0

co-lay



connector to other RTCRST#

RTCRST#\_D 11,34

## tri-state

INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

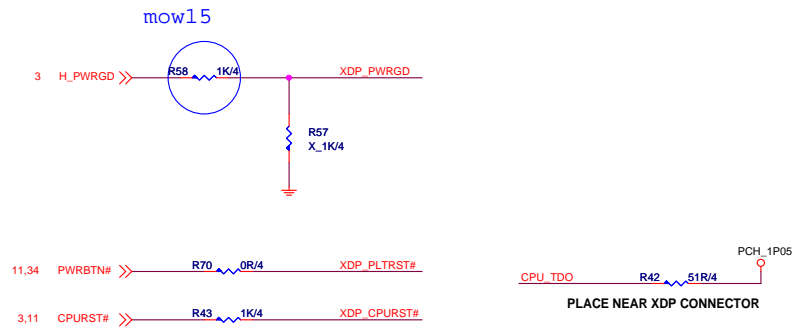
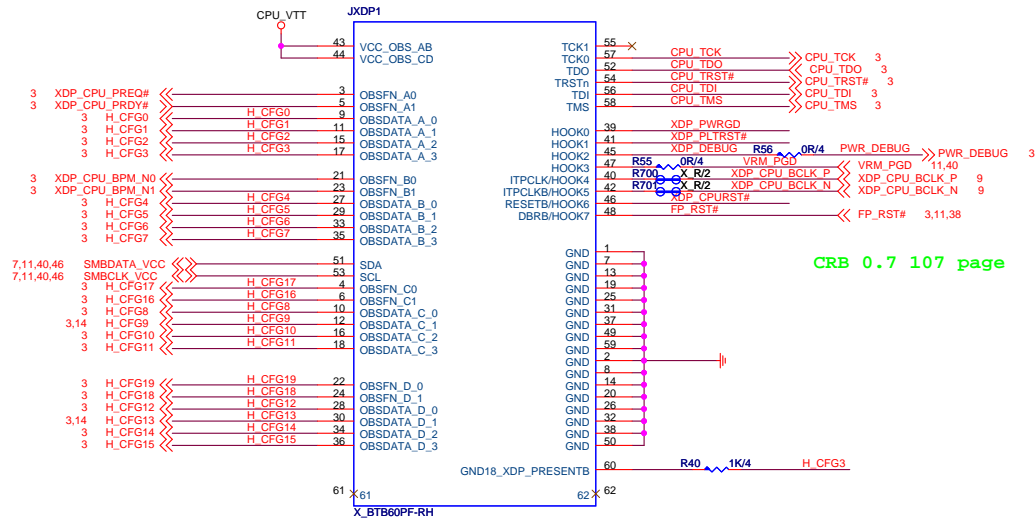


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# **Reserve debug port 5020**



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PD0-0791810-G37,精成,23,寶安恩斯邁廠(MSIS)  
PD0-0791810-G37,精成,77,寶安恩斯邁廠(MSIS)  
PD0-0791810-E48,競華,23,寶安恩斯邁廠(MSIS)  
PD0-0791810-E48,競華,77,寶安恩斯邁廠(MSIS)

SBC\_LA1  
Label  
SBC  
SBC LABEL

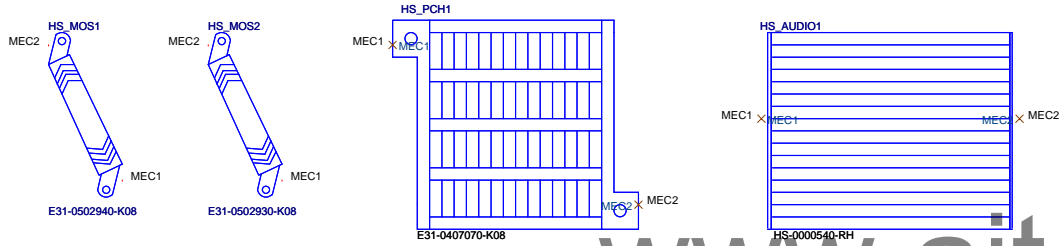
CPU\_H1  
CPU  
鐵座  
CPU\_H1

BAT1\_X1  
BAT-BCR2032P-RH

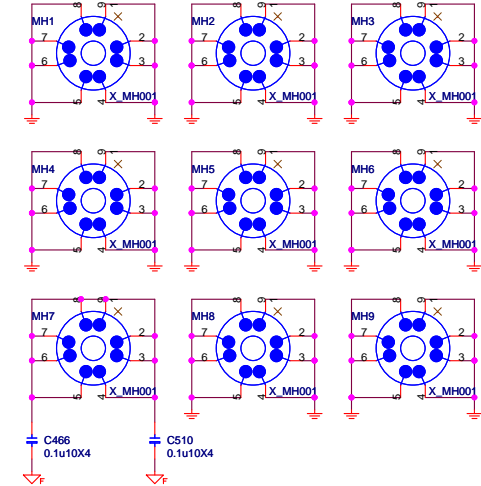
HDMI\_LA1  
Label  
HDMI  
HDMI LABEL

AMI\_LA1  
AMI\_BIOS  
LABEL  
BIOS\_LABEL

## HEATSINK



## Mounting Holes



## SPI OPT.

SPI\_128  
SPI  
SM  
X\_W25Q128FVSIQ-HF

## H97 OPT.

U0H97  
LPT  
H97  
X\_H97  
LAH97  
Label  
H97-Gaming3  
X\_MKT-LABEL

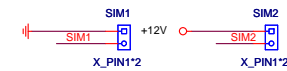
## Z97 OPT.

LAZ97  
Label  
Z97-Gaming3  
MKT-LABEL

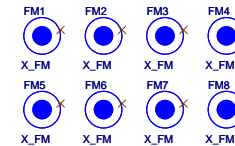
## B85 OPT.

U0B85  
LPT  
B85  
X\_B85  
LAB85  
Label  
B85-Gaming3  
X\_MKT-LABEL  
CNTUSB1  
USB3  
Co-lay  
USB2  
X\_USB2  
NS3-08M0611-P02

## Simulation



## Optical Fiducial Marks-120



## Test point

VCCP		CPU_VCCIN
VCC_DDR		VCC_DDR1
VTT_DDR		VTT_DDR1
PCH_1P05		PCH_CORE1
PCH_1P5		PCH_VCCVRM1
5VDIMM		5VDIMM1
3VSB		3VSB1
VBAT		VBAT1
3VA		3VA1
PCH_VCC3		PCH_VCC1
CPU_VTT		CPU_VCCIO1




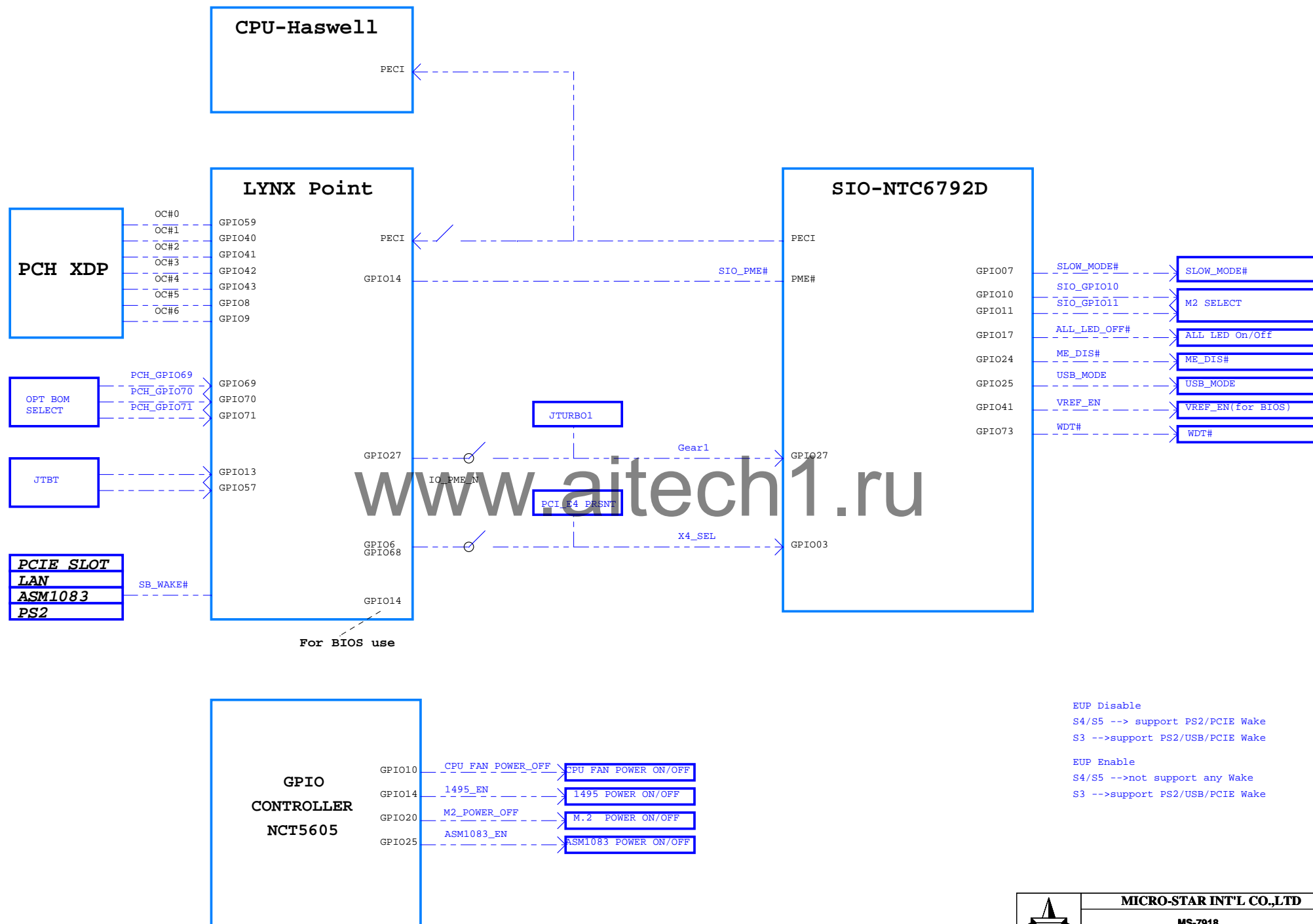
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			<b>MICRO-STAR INT'L CO.,LTD</b>	
			<b>MS-7918</b>	
Size Custom	Document Description <b>EMI CAP</b>			Rev 1.0
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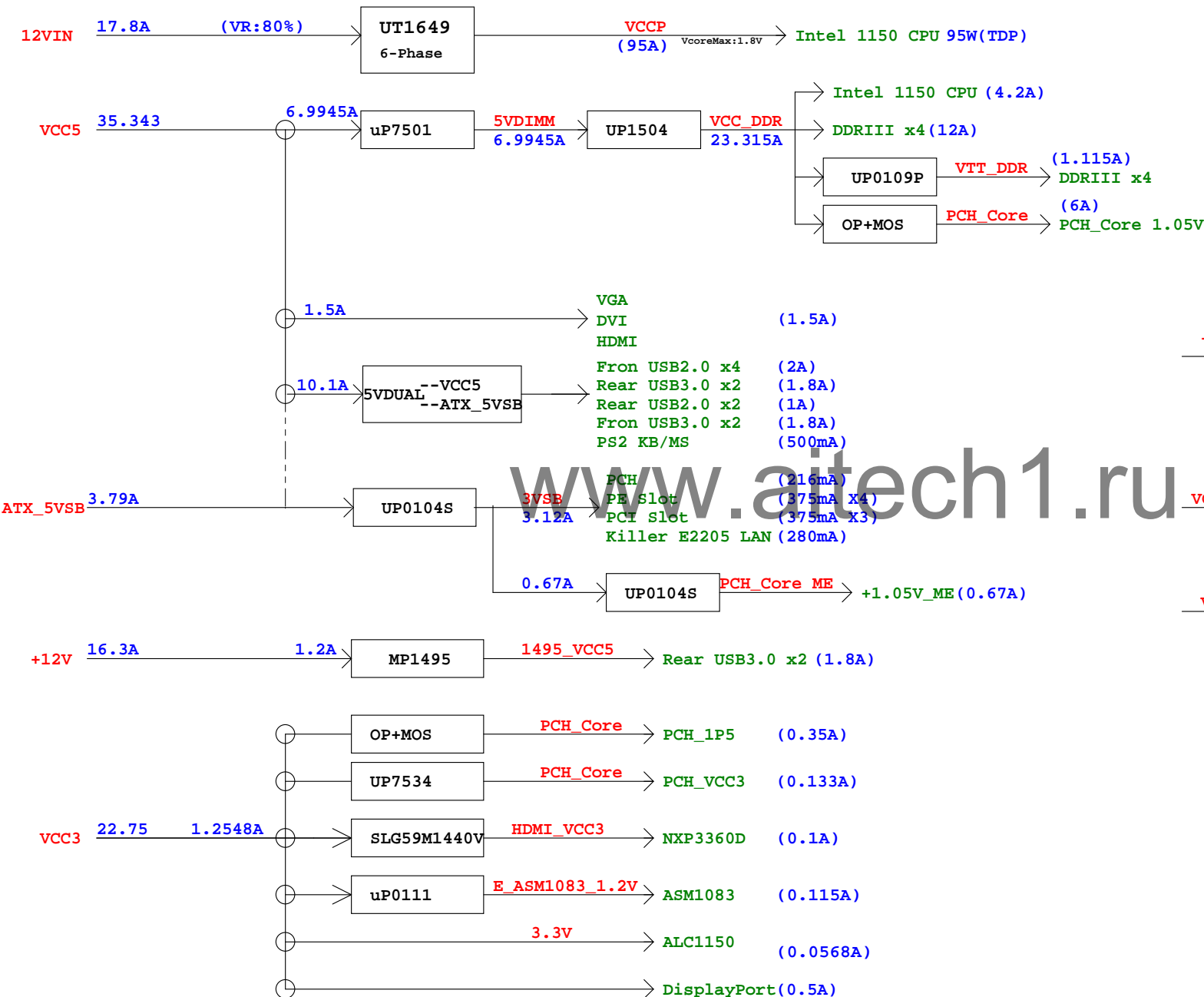


EUP Disable  
 S4/S5 --> support PS2/PCIE Wake  
 S3 -->support PS2/USB/PCIE Wake

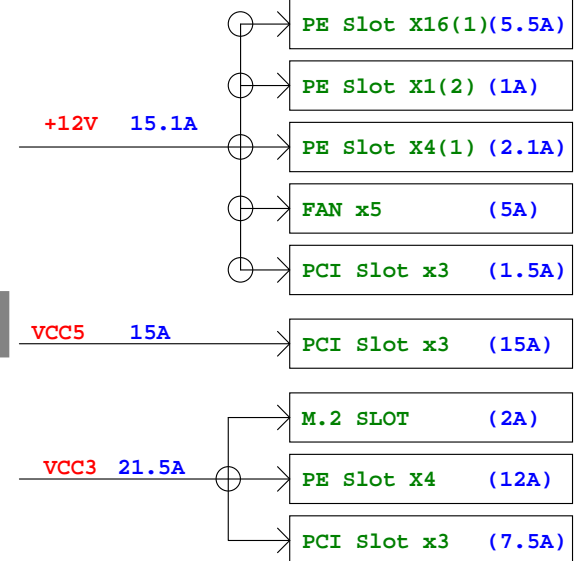
EUP Enable  
 S4/S5 -->not support any Wake  
 S3 -->support PS2/USB/PCIE Wake

# Power Delivery

# Slot



PCI slot (X3)		
+3.3Vaux (wake)	-	1125mA
+3.3Vaux (no wake)	-	60mA
+3.3V	-	7.6A
+5V	-	15A
+12V	-	1.5A



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(G3)DS5 ---> S0

VCCRTC (MB-->PCH)

RTCRST# (MB-->PCH)

SYS3VSB\_OFF (By SIO)

3VSB (By ATX\_5VSB)

RSMRST# (By SIO to PCH) (SIO delay 200ms-300ms as VSB arrives at 3.033V)  
up: 3.033V down:2.882V

PWRBTIN# (to SIO to PCH) (CP Internal 16ms debounce)

SLP\_S5# (By PCH to ???)

SLP\_S4# (By PCH to SIO)

SLP\_S3# (By PCH to SIO)

PSOEN# (as S3) (By SIO to PS) (SIO delay 80ns By SLP\_S3#)

12V/5V/3V (By PS to MB) (12/5V --->3V <=20ms )

5VDRV1 (By S3 & S4 & 5V) (UP7501 delay 6ms-10ms)

5VDIMM (By 5VDRV1)

VCC\_DDR (By 5VDIMM)

VTT\_DDR (By 5V & VCC\_DDR to CPU)

PCH\_1P05 ( by SLP\_S3# & 12V & VCC\_DDR)

PCH\_VCC3 ( by SLP\_S3# & PCH\_1P05)

PCH\_1P5 ( by SLP\_S3#)

VR\_EN (By 12V & SLP\_S3# & PCH\_1P05)

VBOOT (1.7V) (By VR\_EN<=5ms)

VRM\_PGD (VR12.5 to PCH ) (By VBOOT Ready <=100us )

ATX\_PWR\_OK (By PS to SIO 12V/5V/3V Delay 100ms-500ms)

CHIP\_PGDN(SIO\_ATXOK)(SIO to PCH)(By ATX\_PWR\_OK & 3.3V<-2.83V) ( delay 300-500ms)

MEM\_PWRGD (By PCH to CPU) (as CHIP\_PGDN & VR\_READY) ( CPU: 1ms min)

BCLK (as CHIP\_PGDN)

CPUPWROK (PCH to CPU) (By BCLK) MIN 1ms MAX :100ms

VCCIO\_OUT & VCOMP\_OUT (By CPUPWROK)

SVID (VR12 to CPU) (By VR\_EN Ready (>Vih) ) (CPUPWROK delay500us output SVID)

VCCP

VIDALERT# (By SVID Ready )

PLTRST# (PCH to CPU) (By PCH to CPU/SIO) ( CPUPWROK to PLTRST 5ms max)

CPURST# (PCH to CPU) (By PLTRST# )

DMI#

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0A To 1.0

Page 3 Remove PLTRST# Co-lay CPU\_RESET#

Page 5 Add 22u\*7 ON CPU SOCKET BOTTOM Side

page 10 Remove R424 Add R717,R718,R719  
Add R722 For Gear1

Page 11 C348,C349 change to 12P  
R343 un-stuff

Page 17 Remove R447 R448 R467 R517 Q50 Q51  
add R134 R62 R711 R171 R44 R133 Q31 Q5  
For PCI\_E4 X4 SEL Function

Page 20 Add R715,Q42

Page 22 Add C501,R708 For MP1495  
Add Q51,Q91,R713,R647,R720 For OC#0 Level Shift

Page 24 Add C511 For USB Drop

Page 25 Add C502 For MP1495  
Remove R196,R197 For OC#0

Page 29 U11 change to NXP,R141 9.09K,C70,Remove HDMI cut power

Page 31~33 Change CA33,CA45 to -12V\_A

Page 34 CP17,L12 change to 0R/0402  
Change R618 Pull high to SIO\_3VA  
C462 Stuff  
R516 un-stuff  
Add SIO\_GP16 For M.2  
Change GP27 NetName to Gear1

Page 36 Add Fan Cut Power circuit  
R45,R50,Q92,Q93,C756,C757

PAGE 38 R683 Pull-up to PCH\_VCC3  
R682 Pull-up to M2\_VCC3  
R475,R469,Q55 un-stuff  
R483 stuff  
Add D27,D28

Page 39 Q61 Reverse NET 3VSB,VCC3  
Remove 3VA Power Down circuit.  
Remove PEG Co-lay circuit

Page 40 RV87 1.8K  
RV84 1.1K  
RV91,RV51 54.9K  
RV82 499R  
RV49 1K  
RV66 48K  
RV11 Change to 0402  
Add RV115 for Slow Mode


Page 43 R145,C75 Stuff  
Add Q50,R635,R680,C304 for sequence  
Add C465

Page 44 Add C512,R721 For Type 2&3  
U32 Un-stuff  
R436 stuff

Page 46 Add R447,R488 Pull-up to 3VA  
Add R706,R707 for Co-lay GPIO  
Change R677,R679 Pull-up to 3VSB  
Change ESD  
Change U19.3/GPIO10 For Fan cut power

Model	Sample BOM	chipset	Market Name	BIOS Define
MS-7918 10	601-7918-XXX	Z97 chipset	Z97 GAMING 3	E7918ims.2XX
MS-7918 10	601-7918-XXX	H97 chipset	H97 GAMING 3	E7918ims.1XX
MS-7918 10	601-7918-XXX	B85 chipset	B85 GAMING 3	E7918ims.3XX

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